

Colossus 15/17 DIS_OPT Schematic IVY Bridge (rPGA989) Intel PCH (Panther Point)

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**REV:-1
2012-01-05.**

DY:No stuff
DIS_OPT:DISCRTE OPTIMUS installed
DY_35W:No stuff on 35W CPU
DY_45W:No stuff on 45W CPU
CR_Balen17:Stuff for 17"
CR_Goya:Stuff for 15"

<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size
A4

Document Number

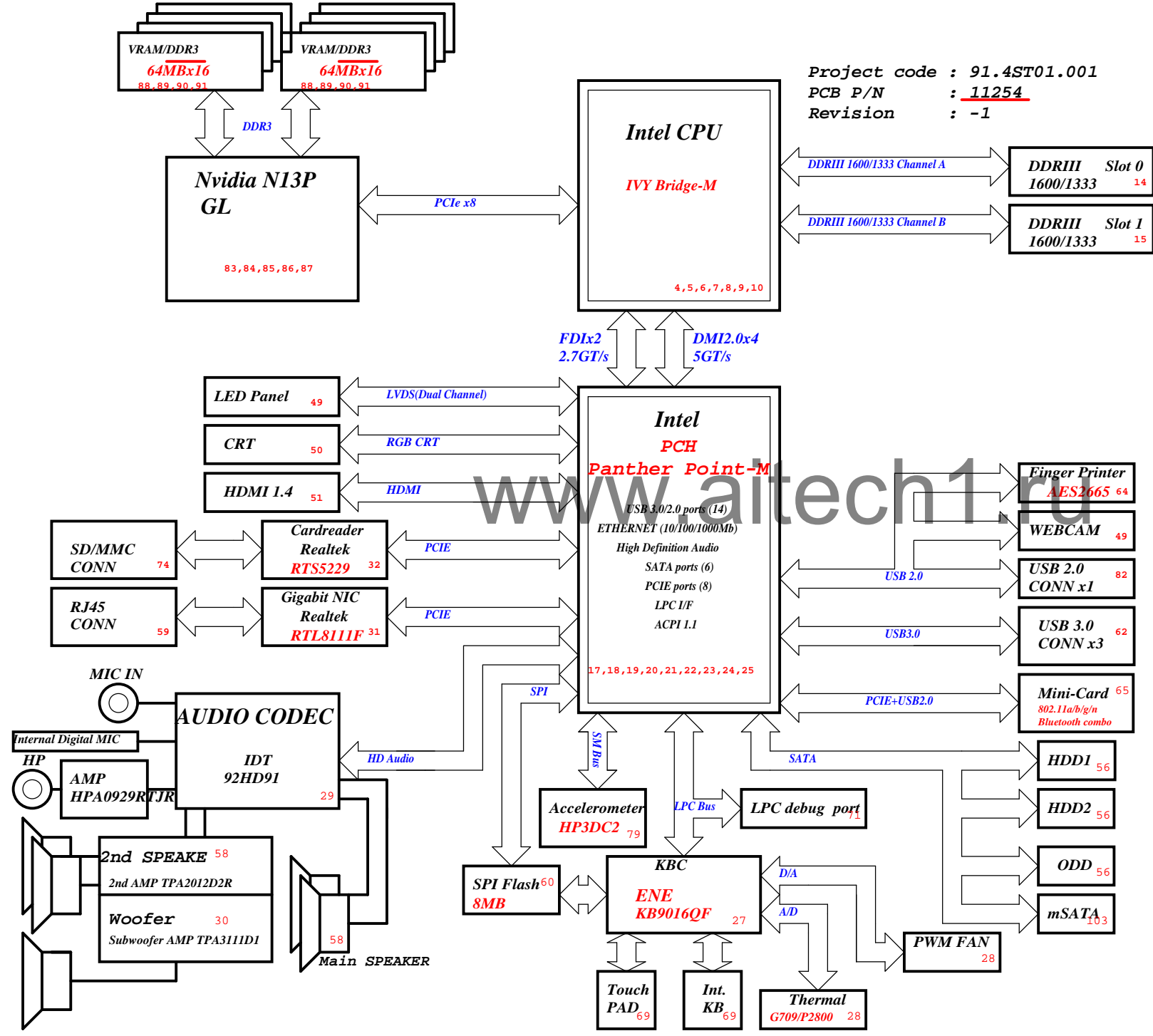
Colossus

Rev
1

Date: Wednesday, January 04, 2012

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COLOSSUS Block Diagram



Project code : 91.4ST01.001
PCB P/N : 11254
Revision : -1

SYSTEM DC/DC TPS51461 48		CPU DC/DC VT1323 42~44	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
5V_S5	VCCSA=0D85V_S0	DCBATOUT (5V_S5)	VCC_CORE

SYSTEM DC/DC SN1003055RUWR 45	
INPUTS	OUTPUTS
5V_S5/3D3V_S5	1D05V_S0

SYSTEM DC/DC RT8223M_5V/3D3V 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC RT8207MZ 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

GFX DC/DC VT1323 42~44	
INPUTS	OUTPUTS
DCBATOUT (5V_S5)	VCC_GFXCORE

VGA NCP3218G 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

CHARGER BQ24738 40	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC RT8068A 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

SYSTEM DC/DC VT385FCX 93	
INPUTS	OUTPUTS
3D3V_S0 1D5V_S0 1D5V_S3	3D3V_VGA_S0 1D5V_VGA_S0 1V05_VGA_S0

Switches 36	
INPUTS	OUTPUTS
1D5V_S3 5V_S5 3D3V_S5	1D5V_S0 5V_S0 3D3V_S0

PCB LAYER (DISCRETE)	
L1:Top L2:GND L3:Signal L4:Signal	L5:VCC L6:Signal L7:GND L8::Bottom

PCH Strapping Chief River Schematic Checklist Rev0.72

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	Enable Danbury: Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. Disable Danbury: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] Disable Danbury: Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low(0) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality. High(1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality. Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

PCIe Routing

LANE1	N/A
LANE2	17"Card Reader
LANE3	15"Card Reader
LANE4	Mini Card1(WLAN)
LANE5	N/A
LANE6	Intel GBE LAN / LAN
LANE7	N/A
LANE8	N/A

USB2.0 Table

Pair	Device
0	USB 3.0 I/O CONN. 1
1	N/A
2	USB 3.0 I/O CONN. 2
3	USB 3.0 I/O CONN. 3
4	FREE
5	BT WLAN combo
6	FREE
7	FREE
8	Fingerprint
9	USB 2.0 I/O CONN.
10	Camera
11	FREE
12	FREE
13	FREE

USB3.0 Table

USB	
Pair	Device
1	I/O CONN. 1
2	FREE
3	I/O CONN. 2
4	I/O CONN. 3

Processor Strapping Chief River Schematic Checklist Rev0.72

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		Disabled - No Physical Display Port attached to 1: Embedded DisplayPort. Enabled - An external Display Port device is 0: connect to the EMBEDDED display Port	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	PEG DEFER TRAINING	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails	
		ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_S0 VCCSA_OD85V OD75V_S0 VCC_CORE VCC_SFPCORE 3D3V_VGA_S0 1D5V_VGA_S0 1D05V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.9 - 0.675V 0.75V 0.35V to 1.5V 0.4 to 1.25V 3.3V 1D5V 1D05V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 ODR_WREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
1D05V_LAN	1.05V	S0/M0, SX/M3	ON whenever iAMT is active
3D3V_M 1D05V_M	3.3V 1.05V	S0/M0, SX/M3, WOL_EN	ON for iAMTLegacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and 3D3V_S5 in Sx

SATA Table

SATA	
Pair	Device
0	HDD1
1	mSATA
2	HDD2
3	N/A
4	ODD
5	N/A

SMBus ADDRESSES

I 2 C / SMBus Addresses		Ref Des	Chief River CRV	
Device			Address	Hex Bus
EC SMBus 1 Battery CHARGER			BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA	
EC SMBus 2 PCH eDP			SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA	
PCH SMBus SO-DIMM (SPD) SO-DIMM (SPD) Digital Pot G-Sensor MINI			PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK	

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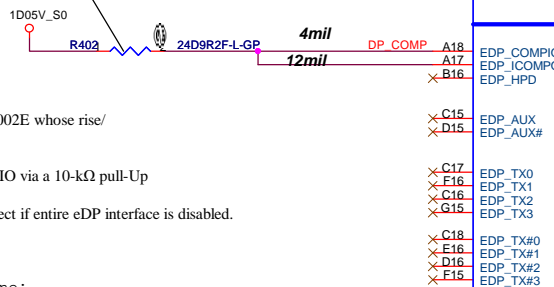
IVY BRIDGE PROCESSOR (DMI,DP,PEG,FDI)

Note:
Intel DMI supports both Lane
Reversal and polarity inversion
but only at PCH side. This is
enabled via a soft strap.

Note:
Intel FDI supports both Lane
Reversal and polarity inversion
but only at PCH side. This is
enabled via a soft strap.

Note:
Lane reversal does not apply to
FDI sideband signals.

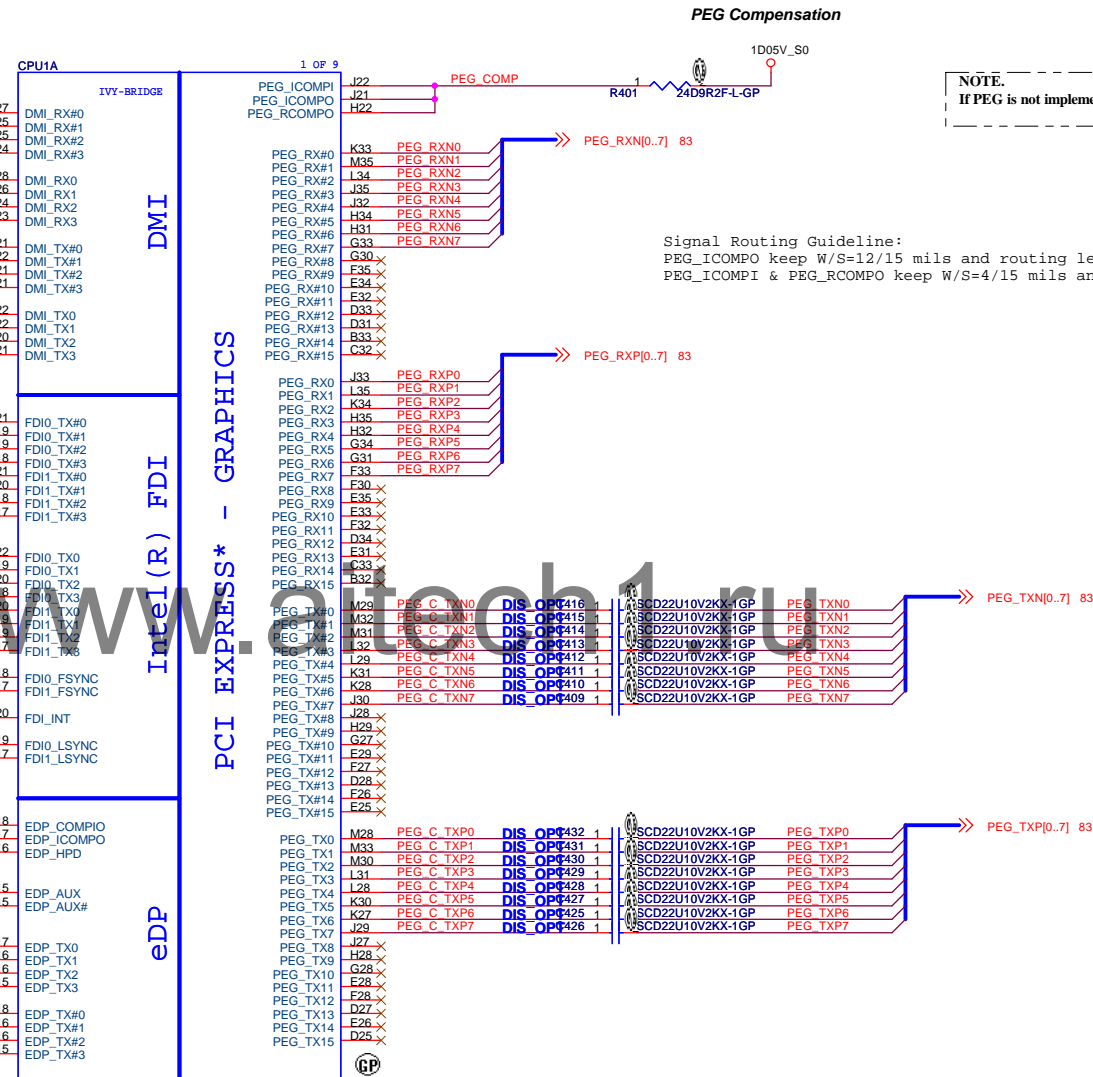
DP Compensation, within 500mil



NOTE: EDP_HPD
Select a Fast FET similar to 2N7002E whose rise/
fall time is less than 6 ns.
If HPD on eDP interface is
disabled, connect it to CPU VCCIO via a 10-k Ω pull-Up
resistor on the motherboard.
This signal can be left as no connect if entire eDP interface is disabled.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing
length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing
length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.



NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

Hand control CPU1 P/N

2ND = 62.10055.321
3RD = 62.10055.551

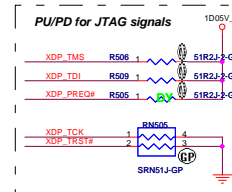
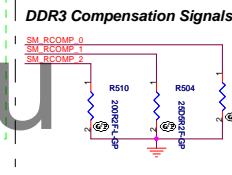
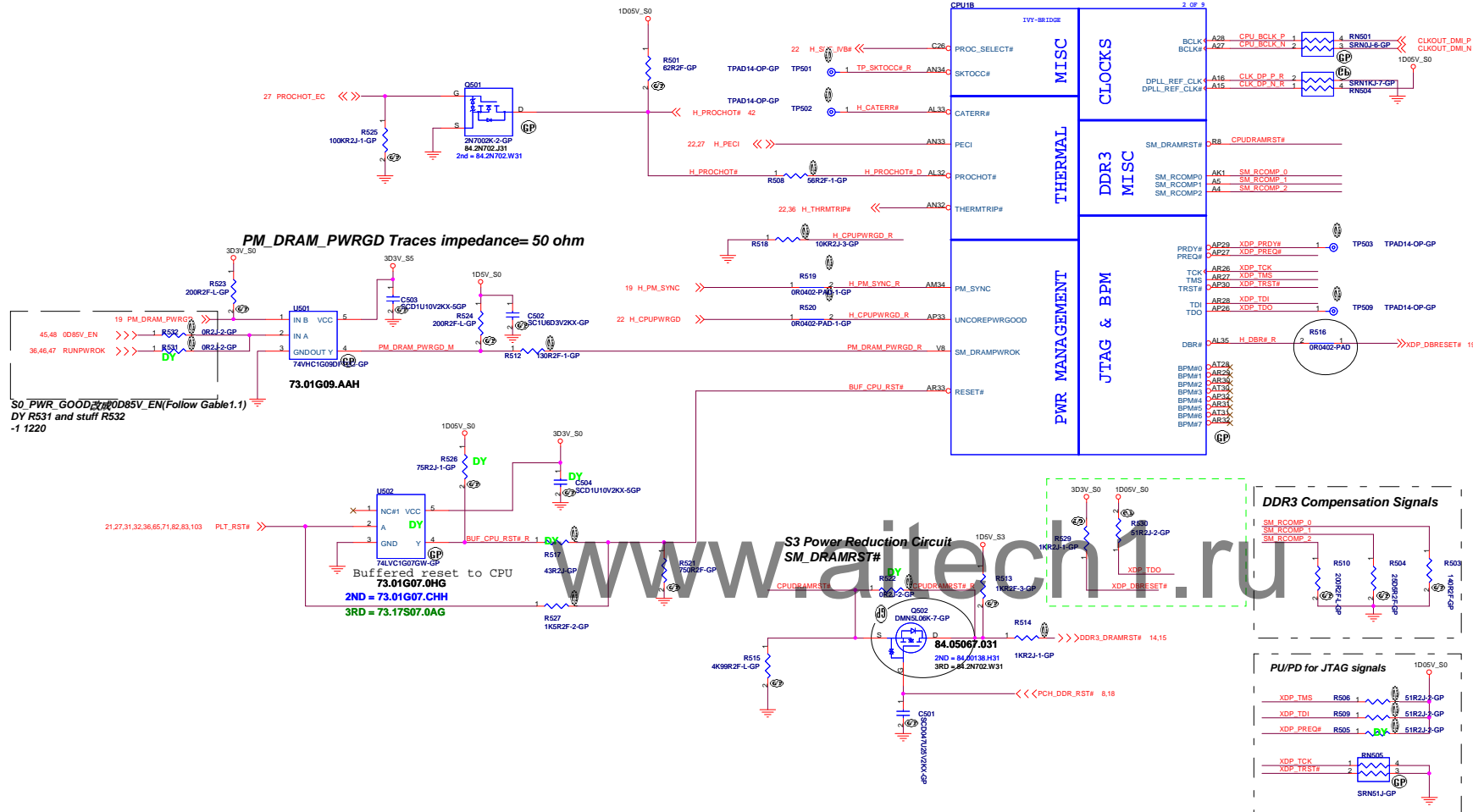
1st 633996-302
2nd 633996-501
3rd 633996-301

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Title			
CPU(1/7): DMI/PEG/FDI			
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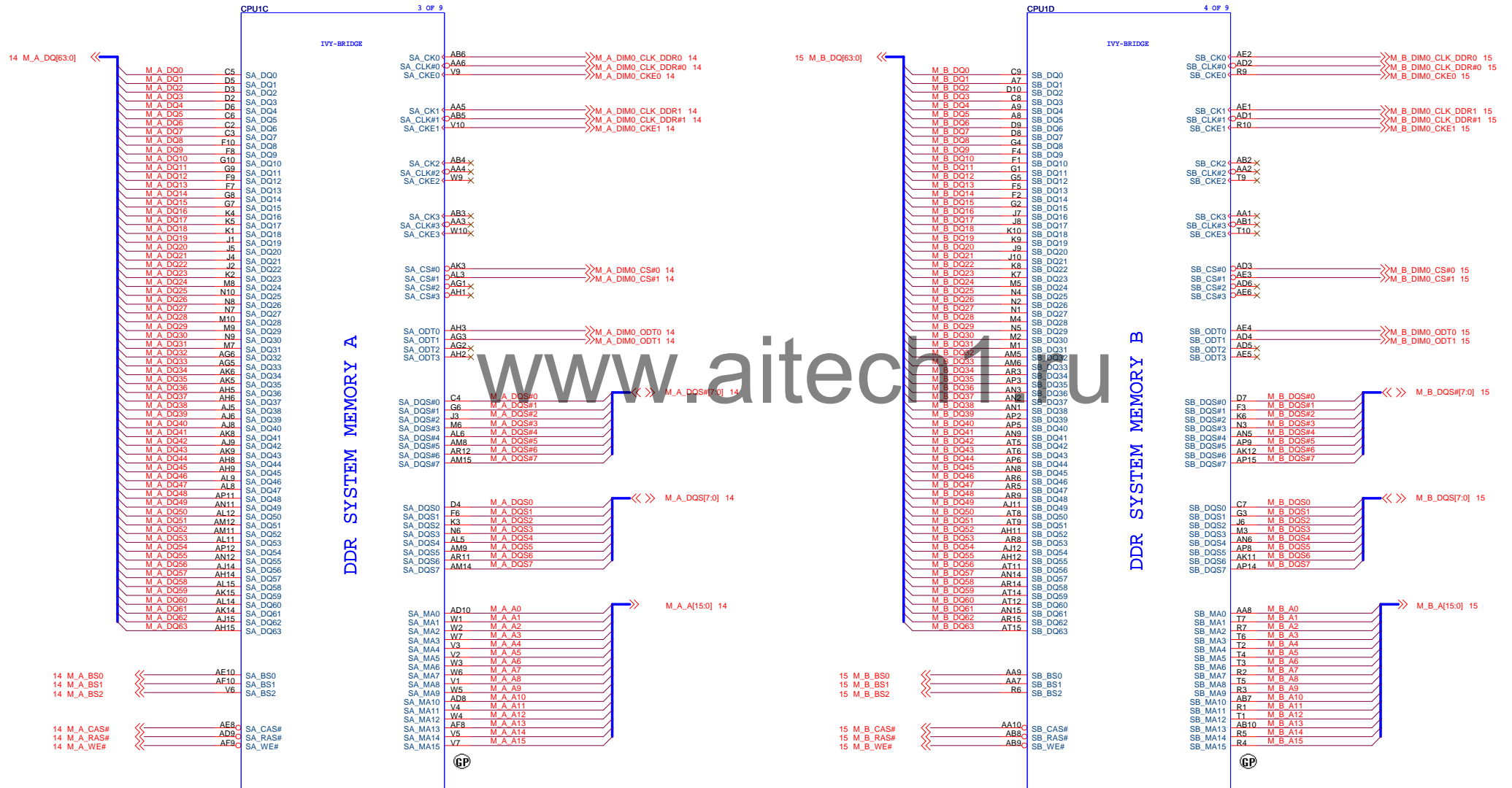
IVY BRIDGE PROCESSOR (CLK,MISC,JTAG)



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CPU(3/7)

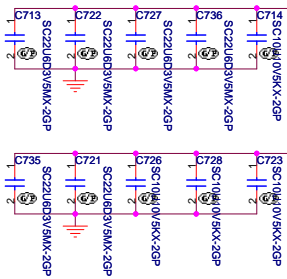
IVY BRIDGE PROCESSOR (DDR3)



CPU(4/7)

IVY BRIDGE PROCESSOR (POWER)

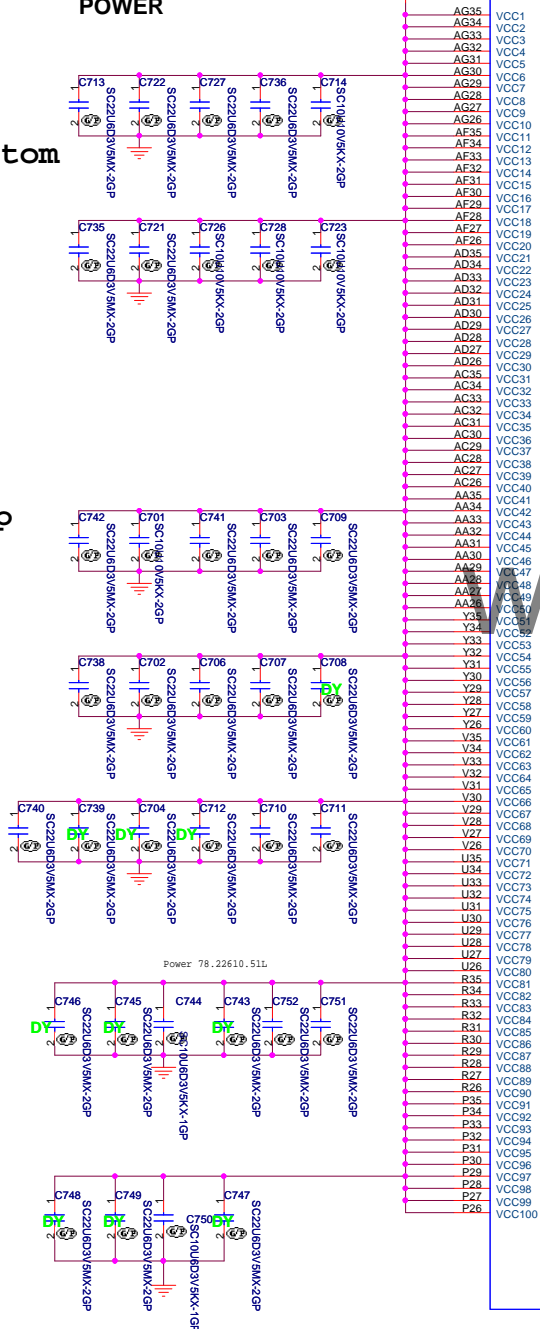
PROCESSOR CORE POWER



Place Bottom

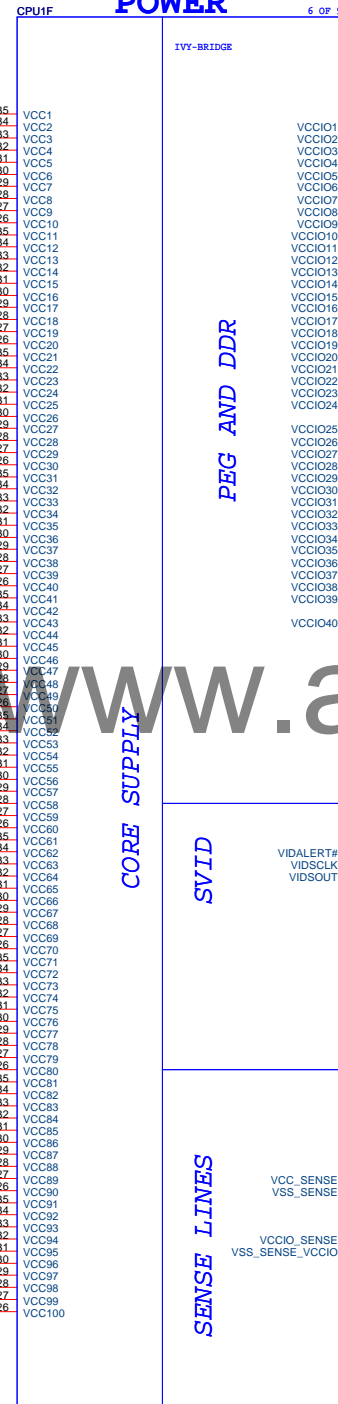
53A
VCC_CORE

Place Top



Power: 78.22610.51L

POWER



CORE SUPPLY

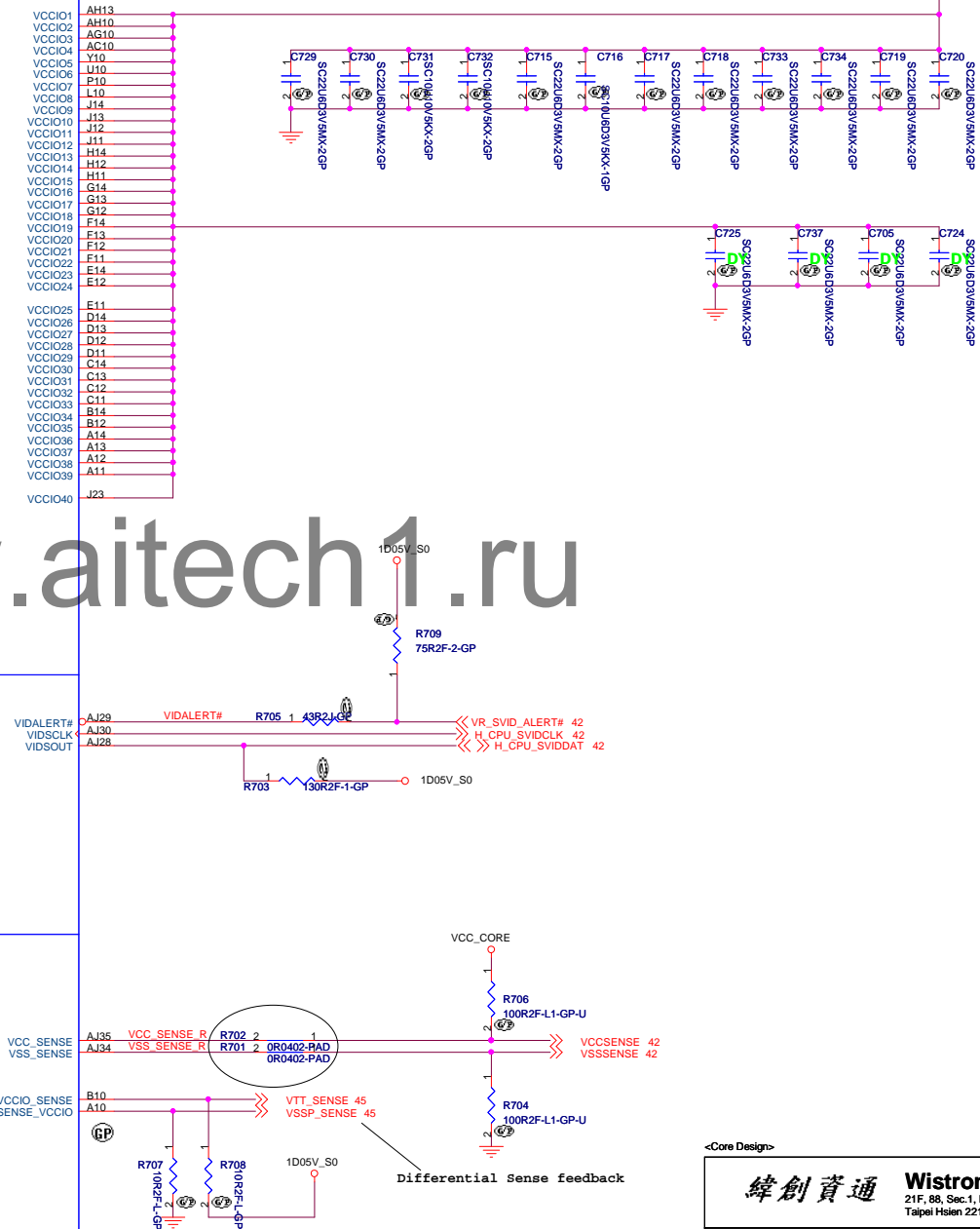
SVID

SENSE LINES

IVY-BRIDGE

PEG AND DDR

PROCESSOR UNCORE POWER

8.5A
1D05V_S0

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Title		
CPU(4/7): PWR		
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CPU(5/7) IVY BRIDGE PROCESSOR (GRAPHICS POWER)

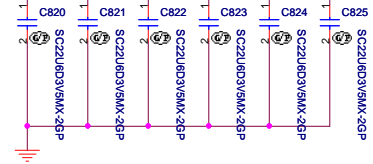
M3 - Processor Generated SO-DIMM VREF_DQ

33A

VCC_GFXCORE 470U*2 22U*6

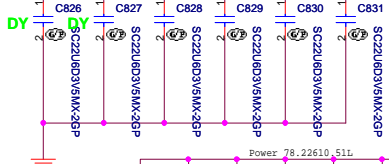
POWER

Under Socket and Closed to CPU

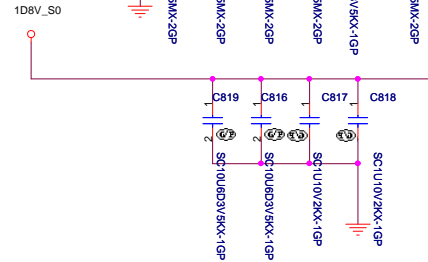


VCC_GFXCORE 22U*6

Closed to CPU Socket



1.5A



CPU1G

IVY-BRIDGE

SENSE LINES

VREF

SM_VREF

SA_DIMM_VREFDQ

SB_DIMM_VREFDQ

DDR3 - 1.5V RAILS

SA RAIL

MISC

1.8V RAIL

VCCSA1

VCCSA2

VCCSA3

VCCSA4

VCCSA5

VCCSA6

VCCSA7

VCCSA8

VCCSA9

VCCSA10

VCCSA11

VCCSA12

VCCSA13

VCCSA14

VCCSA15

VCCSA16

VCCSA17

VCCSA18

VCCSA19

VCCSA20

VCCSA21

VCCSA22

VCCSA23

VCCSA24

VCCSA25

VCCSA26

VCCSA27

VCCSA28

VCCSA29

VCCSA30

VCCSA31

VCCSA32

VCCSA33

VCCSA34

VCCSA35

VCCSA36

VCCSA37

VCCSA38

VCCSA39

VCCSA40

VCCSA41

VCCSA42

VCCSA43

VCCSA44

VCCSA45

VCCSA46

VCCSA47

VCCSA48

VCCSA49

VCCSA50

VCCSA51

VCCSA52

VCCSA53

VCCSA54

VCCSA55

VCCSA56

VCCSA57

VCCSA58

VCCSA59

VCCSA60

VCCSA61

VCCSA62

VCCSA63

VCCSA64

VCCSA65

VCCSA66

VCCSA67

VCCSA68

VCCSA69

VCCSA70

VCCSA71

VCCSA72

VCCSA73

VCCSA74

VCCSA75

VCCSA76

VCCSA77

VCCSA78

VCCSA79

VCCSA80

VCCSA81

VCCSA82

VCCSA83

VCCSA84

VCCSA85

VCCSA86

VCCSA87

VCCSA88

VCCSA89

VCCSA90

VCCSA91

VCCSA92

VCCSA93

VCCSA94

VCCSA95

VCCSA96

VCCSA97

VCCSA98

VCCSA99

VCCSA100

VCCSA101

VCCSA102

VCCSA103

VCCSA104

VCCSA105

VCCSA106

VCCSA107

VCCSA108

VCCSA109

VCCSA110

VCCSA111

VCCSA112

VCCSA113

VCCSA114

VCCSA115

VCCSA116

VCCSA117

VCCSA118

VCCSA119

VCCSA120

VCCSA121

VCCSA122

VCCSA123

VCCSA124

VCCSA125

VCCSA126

VCCSA127

VCCSA128

VCCSA129

VCCSA130

VCCSA131

VCCSA132

VCCSA133

VCCSA134

VCCSA135

VCCSA136

VCCSA137

VCCSA138

VCCSA139

VCCSA140

VCCSA141

VCCSA142

VCCSA143

VCCSA144

VCCSA145

VCCSA146

VCCSA147

VCCSA148

VCCSA149

VCCSA150

VCCSA151

VCCSA152

VCCSA153

VCCSA154

VCCSA155

VCCSA156

VCCSA157

VCCSA158

VCCSA159

VCCSA160

VCCSA161

VCCSA162

VCCSA163

VCCSA164

VCCSA165

VCCSA166

VCCSA167

VCCSA168

VCCSA169

VCCSA170

VCCSA171

VCCSA172

VCCSA173

VCCSA174

VCCSA175

VCCSA176

VCCSA177

VCCSA178

VCCSA179

VCCSA180

VCCSA181

VCCSA182

VCCSA183

VCCSA184

VCCSA185

VCCSA186

VCCSA187

VCCSA188

VCCSA189

VCCSA190

VCCSA191

VCCSA192

VCCSA193

VCCSA194

VCCSA195

VCCSA196

VCCSA197

VCCSA198

VCCSA199

VCCSA200

VCCSA201

VCCSA202

VCCSA203

VCCSA204

VCCSA205

VCCSA206

VCCSA207

VCCSA208

VCCSA209

VCCSA210

VCCSA211

VCCSA212

VCCSA213

VCCSA214

VCCSA215

VCCSA216

VCCSA217

VCCSA218

VCCSA219

VCCSA220

VCCSA221

VCCSA222

VCCSA223

VCCSA224

VCCSA225

VCCSA226

VCCSA227

VCCSA228

VCCSA229

VCCSA230

VCCSA231

VCCSA232

VCCSA233

VCCSA234

VCCSA235

VCCSA236

VCCSA237

VCCSA238

VCCSA239

VCCSA240

VCCSA241

VCCSA242

VCCSA243

VCCSA244

VCCSA245

VCCSA246

VCCSA247

VCCSA248

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VCCSA253

VCCSA254

VCCSA255

VCCSA256

VCCSA257

VCCSA258

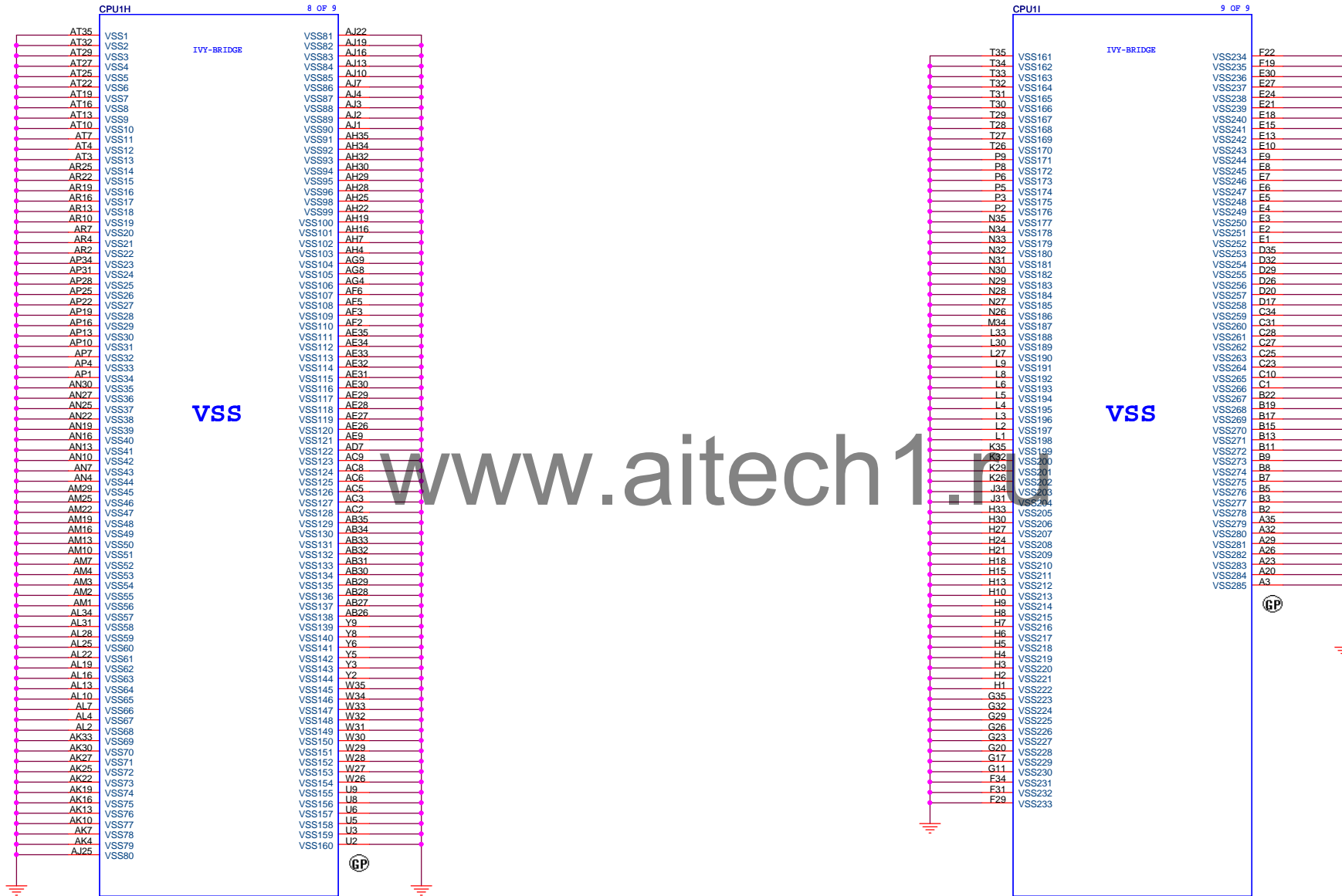
VCCSA259

VCCSA260

VCCSA261

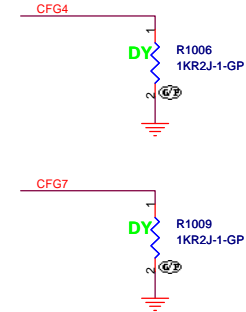
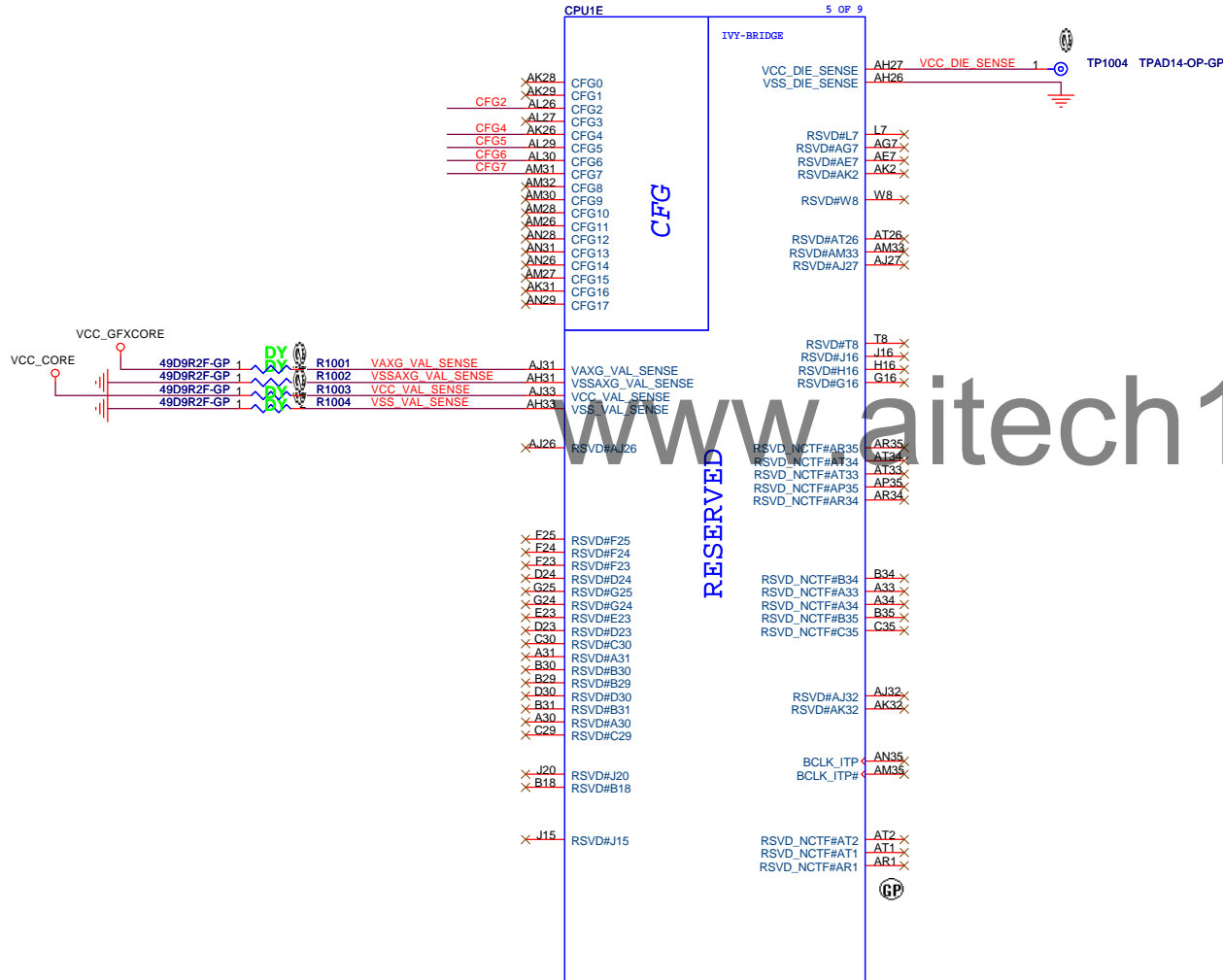
CPU(6/7)

IVY BRIDGE PROCESSOR (GND)



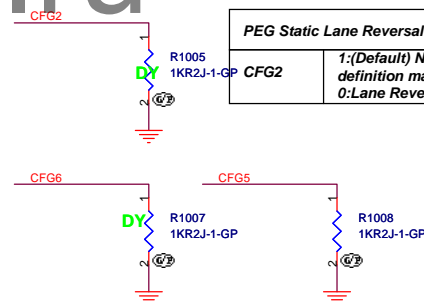
CPU(7/7)

IVY BRIDGE PROCESSOR (RESERVED)



Display Port Presence Strap	
CFG4	1: (Default) Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



PEG Static Lane Reversal	
CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed

PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled; function 2 disabled 01: Reserved - (Device 1 function 1 disabled; function 2 enabled) 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

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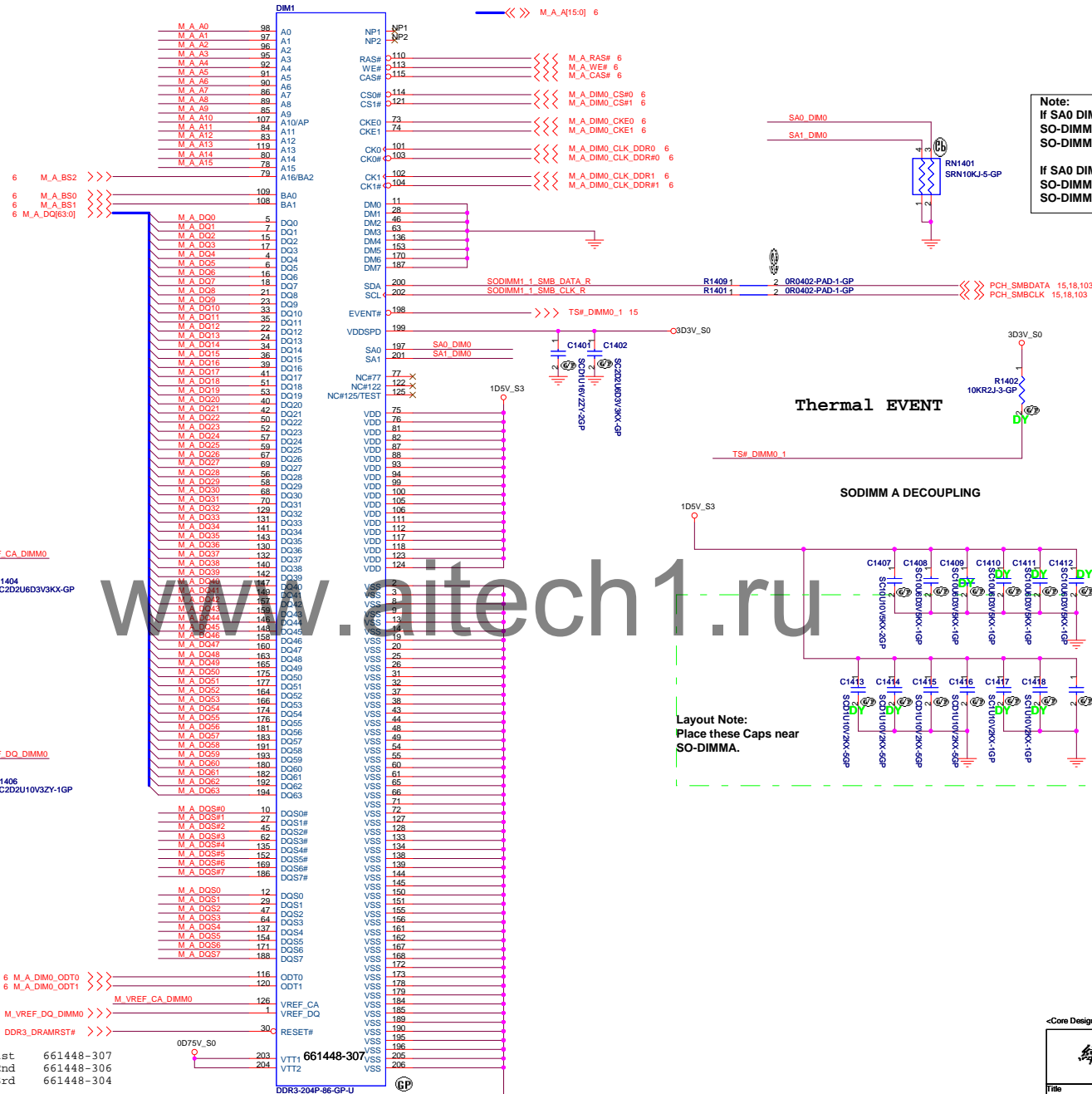
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DIMM1 REVERSED

M_A_DQS#7[7:0] 6
 M_A_DQS#7[7:0] 6
 M_A_A[15:0] 6



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Title **DDR3 SO-DIMM1**
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DIMM2 REVERSED

6 M_B_A[15:0] <<>>
6 M_B_DQS[7:0] <<>>
6 M_B_DQS[7:0] <<>>

6 M_B_BS2 <<>>
6 M_B_BS0
6 M_B_BS1
6 M_B_DQ[63:0]

M_B_A0 96
M_B_A1 97
M_B_A2 98
M_B_A3 99
M_B_A4 100
M_B_A5 101
M_B_A6 102
M_B_A7 103
M_B_A8 104
M_B_A9 105
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M_B_A12 108
M_B_A13 109
M_B_A14 110
M_B_A15 111

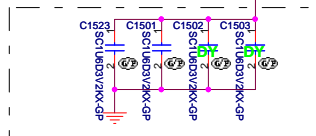
M_B_DQ0 5
M_B_DQ1 6
M_B_DQ2 7
M_B_DQ3 8
M_B_DQ4 9
M_B_DQ5 10
M_B_DQ6 11
M_B_DQ7 12
M_B_DQ8 13
M_B_DQ9 14
M_B_DQ10 15
M_B_DQ11 16
M_B_DQ12 17
M_B_DQ13 18
M_B_DQ14 19
M_B_DQ15 20
M_B_DQ16 21
M_B_DQ17 22
M_B_DQ18 23
M_B_DQ19 24
M_B_DQ20 25
M_B_DQ21 26
M_B_DQ22 27
M_B_DQ23 28
M_B_DQ24 29
M_B_DQ25 30
M_B_DQ26 31
M_B_DQ27 32
M_B_DQ28 33
M_B_DQ29 34
M_B_DQ30 35
M_B_DQ31 36
M_B_DQ32 37
M_B_DQ33 38
M_B_DQ34 39
M_B_DQ35 40
M_B_DQ36 41
M_B_DQ37 42
M_B_DQ38 43
M_B_DQ39 44
M_B_DQ40 45
M_B_DQ41 46
M_B_DQ42 47
M_B_DQ43 48
M_B_DQ44 49
M_B_DQ45 50
M_B_DQ46 51
M_B_DQ47 52
M_B_DQ48 53
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M_B_DQ50 55
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M_B_DQ57 62
M_B_DQ58 63
M_B_DQ59 64
M_B_DQ60 65
M_B_DQ61 66
M_B_DQ62 67
M_B_DQ63 68

M_B_DQS#0 10
M_B_DQS#1 27
M_B_DQS#2 45
M_B_DQS#3 63
M_B_DQS#4 81
M_B_DQS#5 99
M_B_DQS#6 117
M_B_DQS#7 135

M_B_DQS0 12
M_B_DQS1 29
M_B_DQS2 47
M_B_DQS3 65
M_B_DQS4 83
M_B_DQS5 101
M_B_DQS6 119
M_B_DQS7 137

6 M_B_DIM0_ODT0 <<>>
6 M_B_DIM0_ODT1 <<>>
M_VREF_CA_DIMM1 <<>>
8 M_VREF_DQ_DIMM1 <<>>
5,14 DDR3_DRAMRST# <<>>

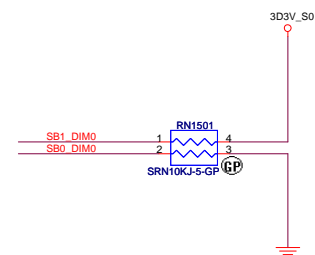
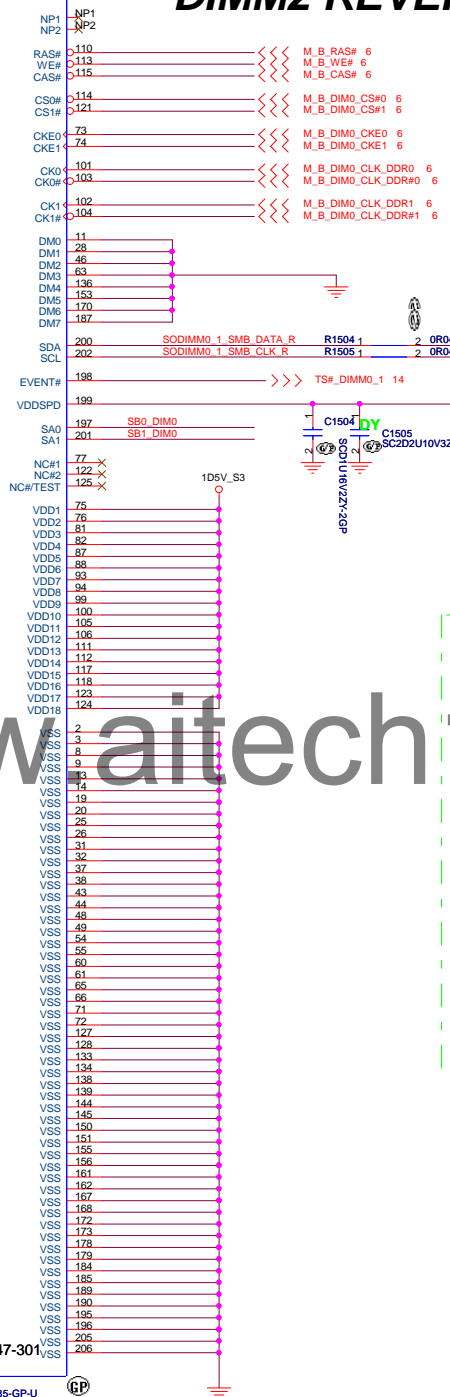
Place these caps close to VTT1 and VTT2.



1st 661447-301
2nd 661447-306
3rd 661447-304

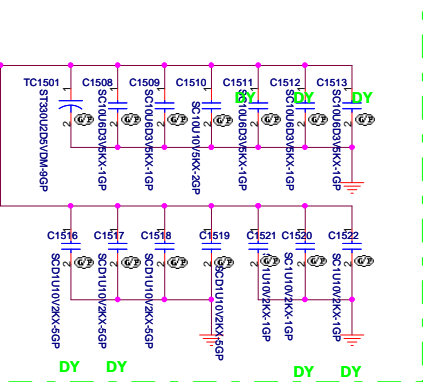
010412 Update connector HP P/N,
hanle control but not change library

62.10017.U21
2ND = 62.10017.T91
3rd = 62.10024.I61
H=5.2mm



Note:
SO-DIMM SPD Address is 0x44
SO-DIMM TS Address is 0x34

SODIMM B DECOUPLING



Layout Note:
Place these Caps near SO-DIMM.

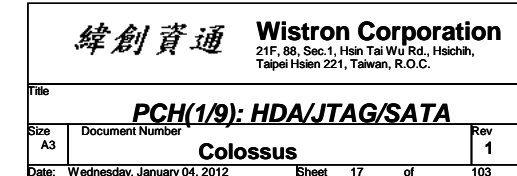
<Core Design>

緯創資通 Wistron Corporation 2/F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
DDR3 SO-DIMM2	
Size	Document Number
Custom	Colossus
Date: Wednesday, January 04, 2012	Sheet 15 of 103

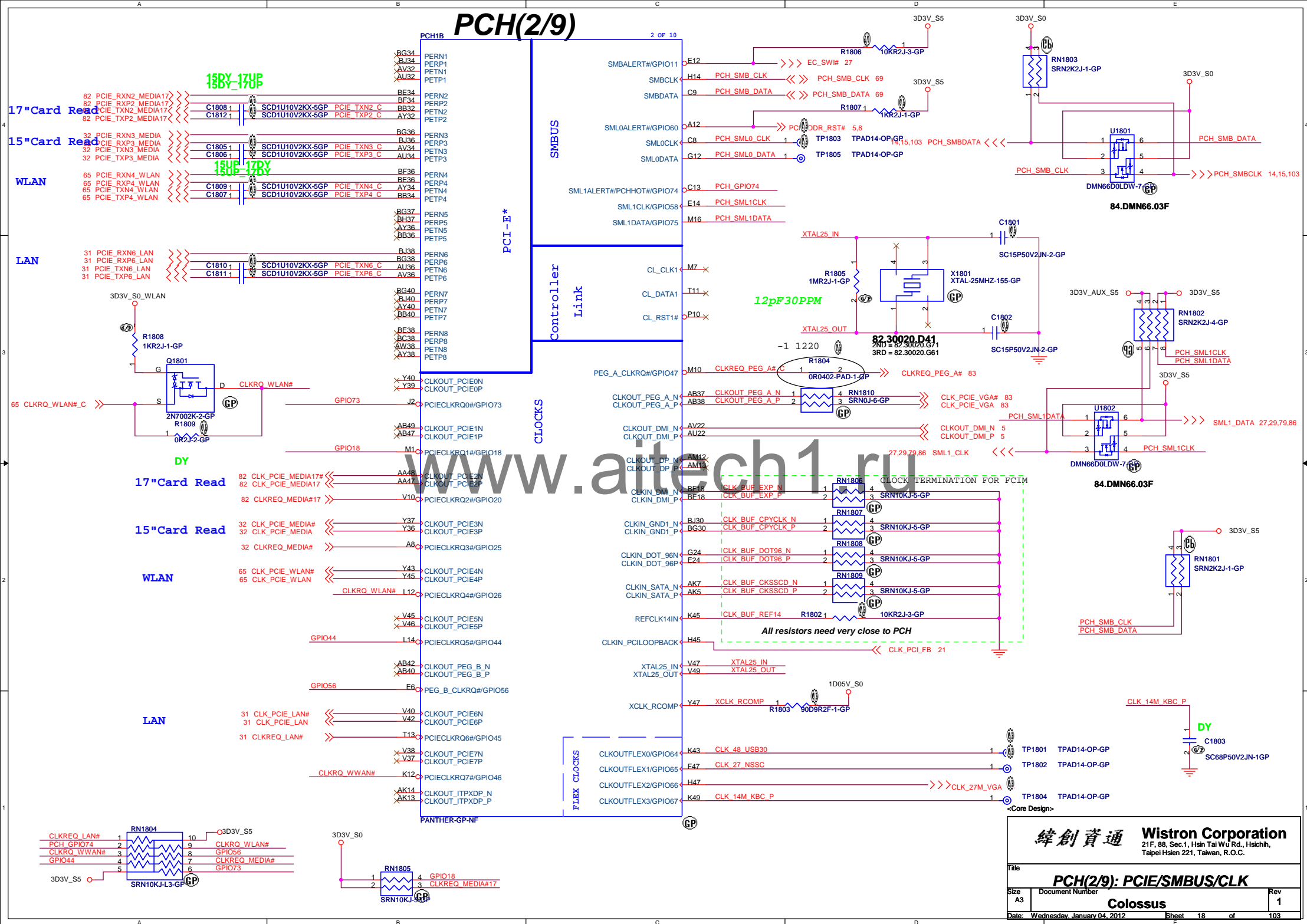
(Blanking)

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INTVRMEN- Integrated
SUS 1.05V VRM Enable
High - Enable internal VRs

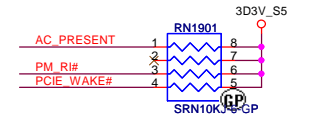


PCH1B 2 OF 10



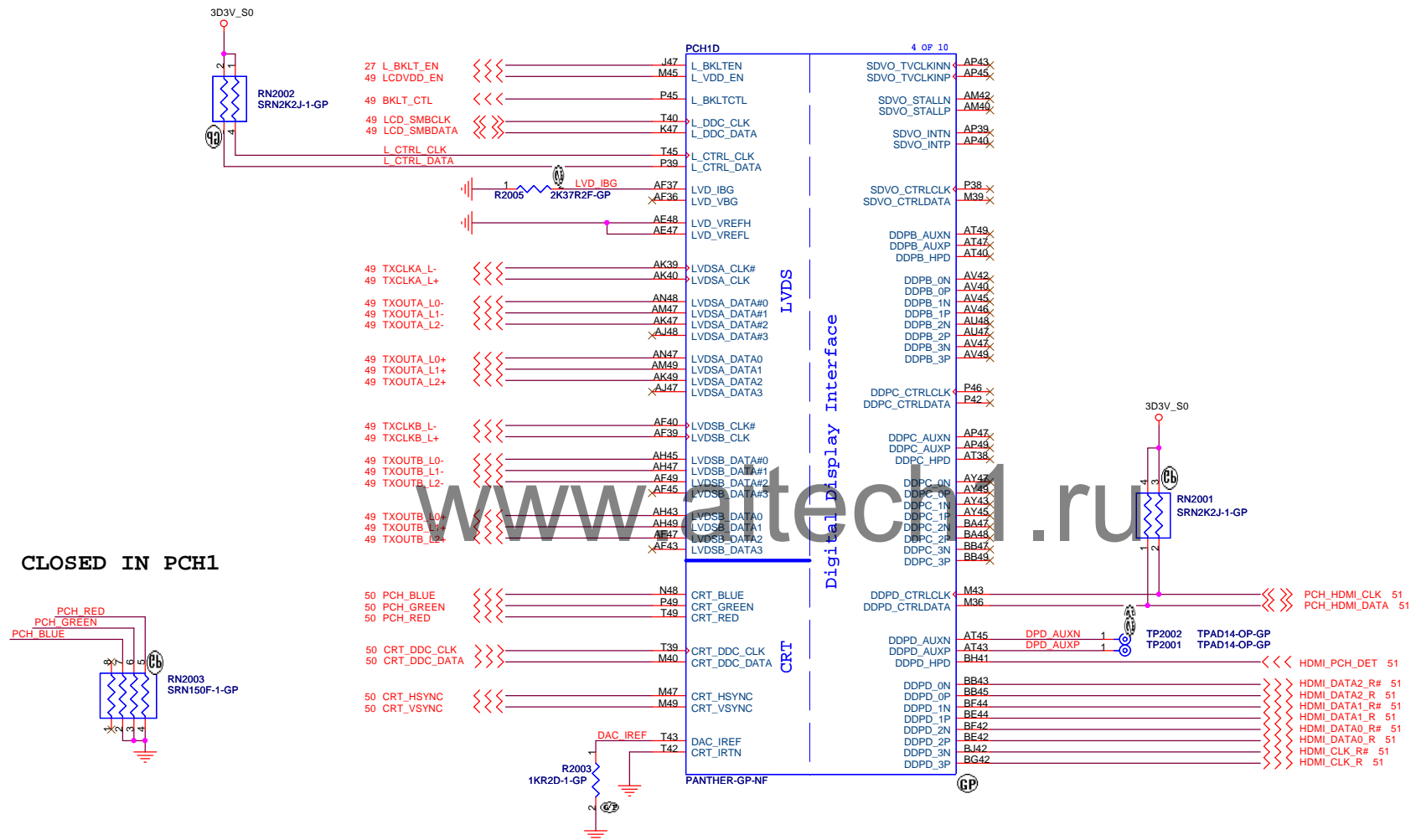
DSWODVREN - On Die DSW VR Enable	
HIGH (R1917 STUFFED, R1901 UNSTUFFED)	Enabled (DEFAULT)
LOW (R1917 UNSTUFFED, R1901 STUFFED)	Disabled

The diagram illustrates the connection of the DSWODVREN signal to the RTC_AUX_S5 pin. The DSWODVREN signal is connected to the R1901 pin (1), which is connected to the R1917 pin (1). The R1917 pin (1) is connected to the RTC_AUX_S5 pin through a 330K resistor. The RTC_AUX_S5 pin is also connected to the RTC_AUX_S5 pin through a 330K resistor. The RTC_AUX_S5 pin is connected to ground through a diode (DY).



Signal Name	Platform With M3 Support (e.g., Intel AMT)	Platform Without M3 Support
SUSPWRDNACK(GPIO30)	Required	Required
ACPRESENT(GPIO31)	Required	Required
SLP_A#	Required	(Tie to SLP_S3#) Note: If SLP_S3# is not routed from PCH to EC, then SLP_A# becomes required from Intel ME-EC prespecprive.

PCH(4/9)



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Title

PCH(4/9): LVDS/CRT/DDI

Size

Document Number	
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Colossus

Rev

Date: Wednesday, January 04, 2012

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PCH(5/9)

USB2.0 Table

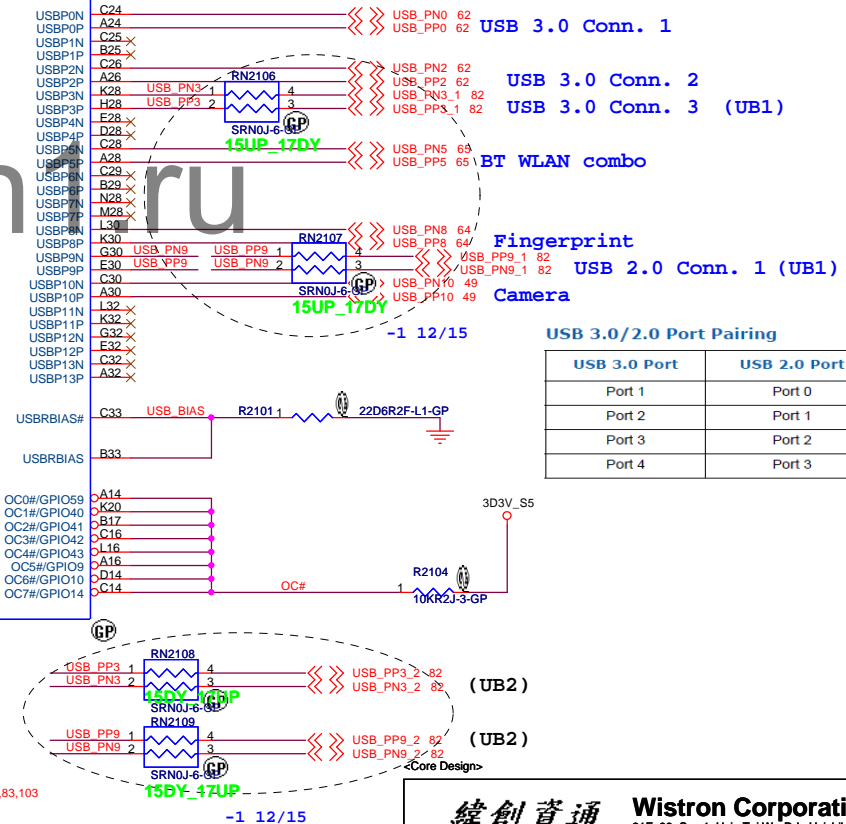
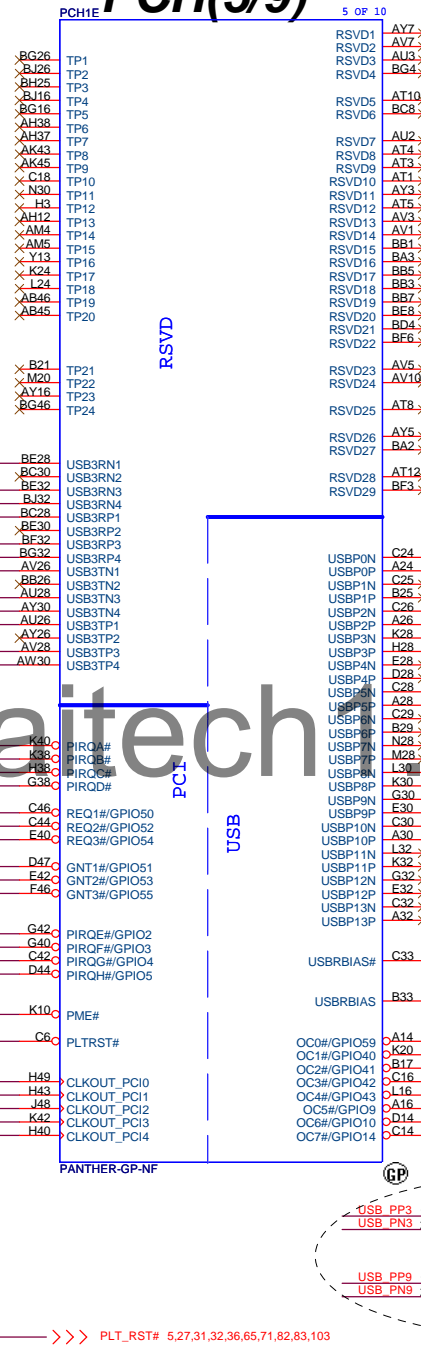
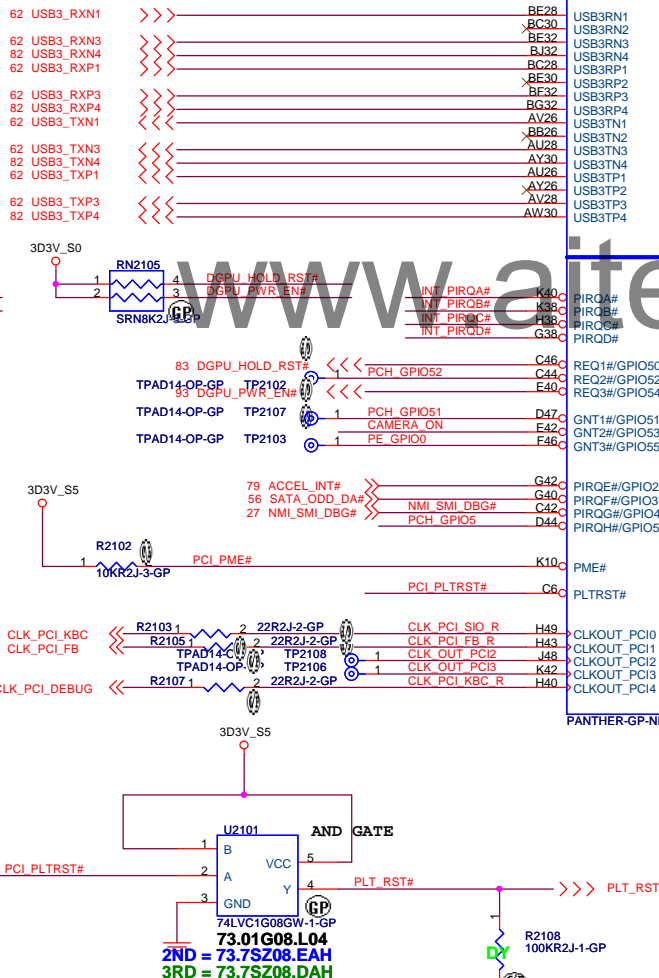
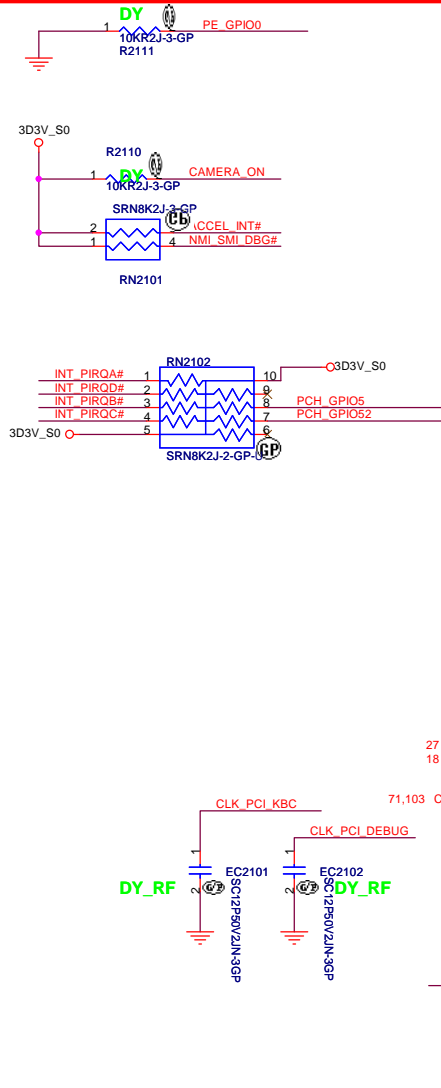
USB	
Pair	Device
0	USB 3.0 I/O CONN.
1	N/A
2	USB 3.0 I/O CONN.
3	USB 3.0 I/O CONN.
4	FREE
5	BT WLAN combo
6	FREE
7	FREE
8	Fingerprint
9	USB 2.0 CONN(Debug)
10	Camera
11	FREE
12	FREE
13	FREE

USB3.0 Table

USB	
Pair	Device
1	I/O CONN. 1 LEFT_DOWN
2	FREE
3	I/O CONN. 2 LEFT_UP
4	I/O CONN. 3 RIGHT_UP

BOOT BIOS Strap

BOOT BIOS Strap		
GNT1#/ <u>GPIO51</u>	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)



USB 3.0/2.0 Port Pairing

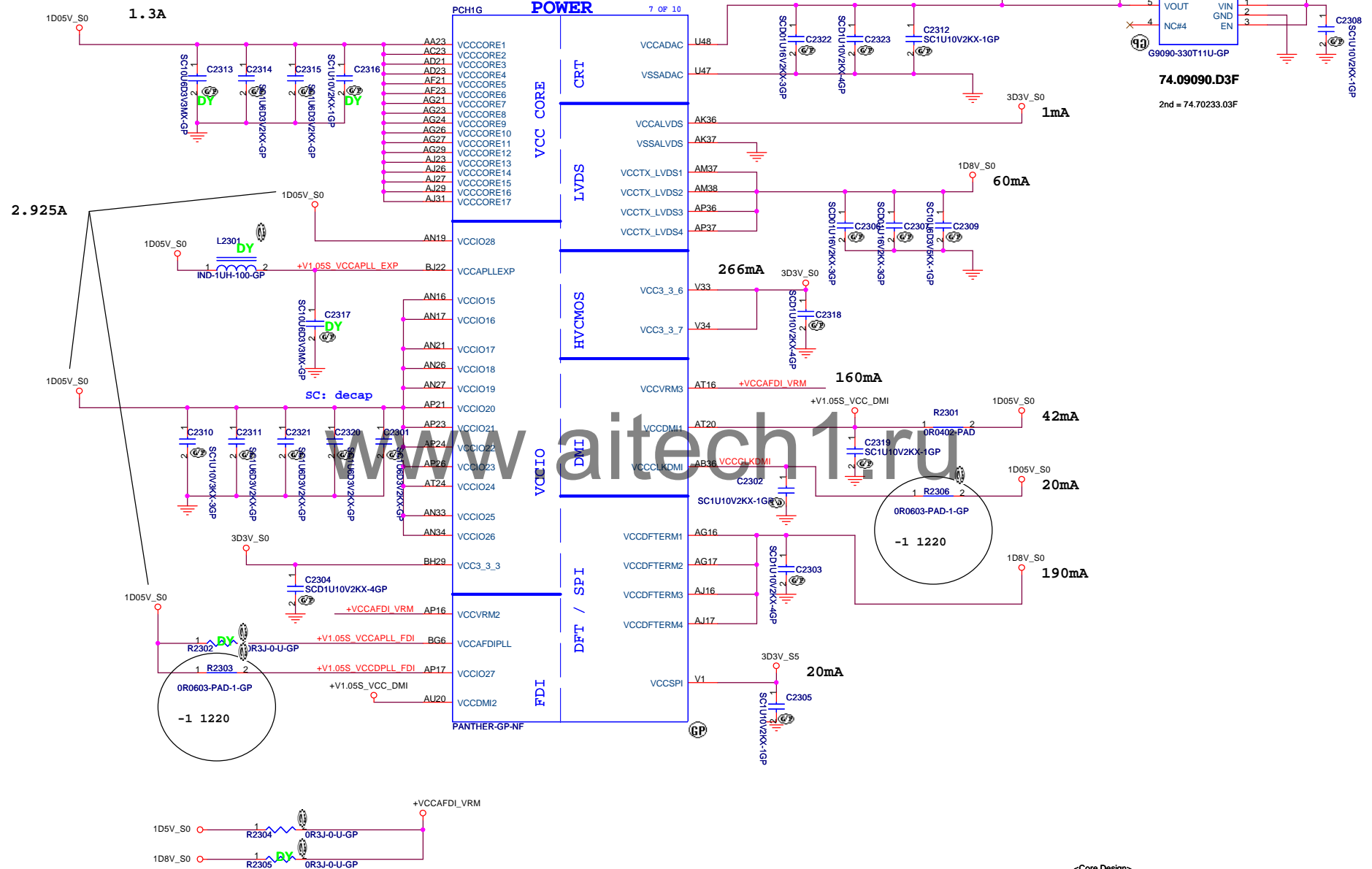
USB 3.0 Port	USB 2.0 Port
Port 1	Port 0
Port 2	Port 1
Port 3	Port 2
Port 4	Port 3

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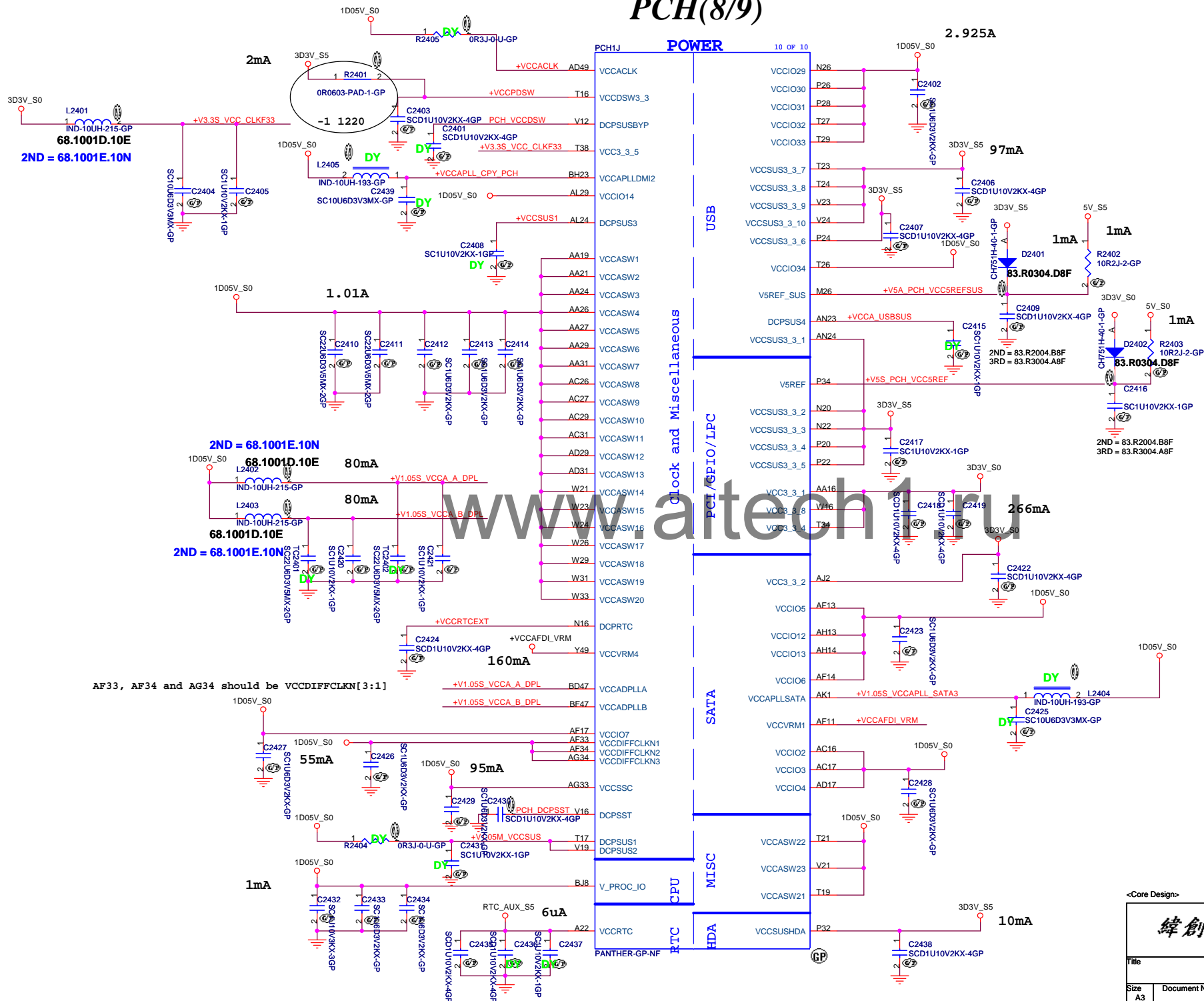
Title			
PCH(5/9): PCI/USB/NVM			
Size A3	Document Number		Rev
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Date:	Wednesday, January 04, 2012	Sheet 21 of	103

VCC_PCH: 6A

PCH(7/9)



PCH(8/9)



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Title			PCH(8/9): PWR2	
Size	Document Number	Rev		1
A3	Colossus			
Date:	Tuesday, December 27, 2011	Sheet	24	of 103

PCH(9/9)

PCH11		9 OF 10	
AY4	VSS159	VSS259	H46
AY42	VSS160	VSS260	K18
AY46	VSS161	VSS261	K26
AY8	VSS162	VSS262	K39
B11	VSS163	VSS263	K46
B15	VSS164	VSS264	K7
B19	VSS165	VSS265	L18
B23	VSS166	VSS266	L2
B27	VSS167	VSS267	L20
B31	VSS168	VSS268	L26
B35	VSS169	VSS269	L28
B39	VSS170	VSS270	L36
B7	VSS171	VSS271	L48
F45	VSS172	VSS272	M12
BB12	VSS173	VSS273	P16
BB16	VSS174	VSS274	M18
BB20	VSS175	VSS275	M22
BB22	VSS176	VSS276	M24
BB24	VSS177	VSS277	M30
BB28	VSS178	VSS278	M32
BB30	VSS179	VSS279	M34
BB38	VSS180	VSS280	M38
BB4	VSS181	VSS281	M4
BB46	VSS182	VSS282	M42
BC14	VSS183	VSS283	M46
BC18	VSS184	VSS284	M8
BC2	VSS185	VSS285	N18
BC22	VSS186	VSS286	P30
BC26	VSS187	VSS287	N47
BC32	VSS188	VSS288	P18
BC34	VSS189	VSS289	T33
BC36	VSS190	VSS290	P40
BC40	VSS191	VSS291	P43
BC42	VSS192	VSS292	P47
BC48	VSS193	VSS293	P7
BD46	VSS194	VSS294	R2
BD5	VSS195	VSS295	R48
BE22	VSS196	VSS296	T12
BE26	VSS197	VSS297	T31
BE40	VSS198	VSS298	T37
BE10	VSS199	VSS299	T4
BE12	VSS200	VSS300	W34
BE16	VSS201	VSS301	T46
BE20	VSS202	VSS302	T47
BE22	VSS203	VSS303	T8
BE24	VSS204	VSS304	V11
BE26	VSS205	VSS305	V17
BE28	VSS206	VSS306	V26
BD3	VSS207	VSS307	V27
BF30	VSS208	VSS308	V29
BF38	VSS209	VSS309	V3
BF40	VSS210	VSS310	V36
BF8	VSS211	VSS311	V38
BG17	VSS212	VSS312	V43
BG21	VSS213	VSS313	V7
BG33	VSS214	VSS314	W17
BG44	VSS215	VSS315	W19
BG8	VSS216	VSS316	W2
BH11	VSS217	VSS317	W27
BH15	VSS218	VSS318	W48
BH17	VSS219	VSS319	X12
BH19	VSS220	VSS320	Y38
H10	VSS221	VSS321	Y4
BH27	VSS222	VSS322	Y42
BH31	VSS223	VSS323	Y46
BH33	VSS224	VSS324	Y8
BH35	VSS225	VSS325	BG29
BH39	VSS226	VSS328	N24
BH43	VSS227	VSS329	AJ3
BH7	VSS228	VSS330	AD47
D3	VSS229	VSS331	B43
D12	VSS230	VSS333	BE10
D16	VSS231	VSS334	BG41
D18	VSS232	VSS335	G14
D22	VSS233	VSS337	H16
D24	VSS234	VSS338	T36
D26	VSS235	VSS340	BG22
D30	VSS236	VSS342	BG24
D32	VSS237	VSS343	C22
D34	VSS238	VSS344	AP13
D38	VSS239	VSS345	M14
D42	VSS240	VSS346	AP3
D8	VSS241	VSS347	AP1
E18	VSS242	VSS348	BE16
E26	VSS243	VSS349	BC16
G18	VSS244	VSS350	BG28
G20	VSS245	VSS351	GJ28
G26	VSS246	VSS352	
G28	VSS247		
G36	VSS248		
G48	VSS249		
H12	VSS250		
H18	VSS251		
H22	VSS252		
H24	VSS253		
H26	VSS254		
H30	VSS255		
H32	VSS256		
H34	VSS257		
F3	VSS258		

PCH1H		8 OF 10	
H5	VSS0		
AA17	VSS1	VSS80	AK38
AA2	VSS2	VSS81	AK4
AA3	VSS3	VSS82	AK42
AA33	VSS4	VSS83	AK46
AA34	VSS5	VSS84	AK8
AB11	VSS6	VSS85	AL16
AB14	VSS7	VSS86	AL17
AB39	VSS8	VSS87	AL19
AB4	VSS9	VSS88	AL2
AB5	VSS10	VSS89	AL21
AB7	VSS11	VSS90	AL23
AC19	VSS12	VSS91	AL26
AC2	VSS13	VSS92	AL27
AC21	VSS14	VSS93	AL31
AC24	VSS15	VSS94	AL33
AC33	VSS16	VSS95	AL34
AC34	VSS17	VSS96	AM11
AC48	VSS18	VSS97	AM14
AD10	VSS19	VSS98	AM16
AD11	VSS20	VSS99	AM36
AD12	VSS21	VSS100	AM39
AD13	VSS22	VSS101	AM43
AD19	VSS23	VSS102	AM45
AD24	VSS24	VSS103	AM46
AD26	VSS25	VSS104	AM7
AD27	VSS26	VSS105	AN2
AD33	VSS27	VSS106	AN29
AD34	VSS28	VSS107	AN3
AD36	VSS29	VSS108	AN31
AD37	VSS30	VSS109	AP12
AD38	VSS31	VSS110	AP19
AD39	VSS32	VSS111	AP28
AD4	VSS33	VSS112	AP30
AD40	VSS34	VSS113	AP32
AD42	VSS35	VSS114	AP38
AD43	VSS36	VSS115	AP4
AD45	VSS37	VSS116	AP42
AD46	VSS38	VSS117	AP46
AD8	VSS39	VSS118	AP8
AE2	VSS40	VSS119	AR2
AE3	VSS41	VSS120	AR48
AE10	VSS42	VSS121	AT11
AE12	VSS43	VSS122	AT13
AE14	VSS44	VSS123	AT18
AE16	VSS45	VSS124	AT22
AE19	VSS46	VSS125	AT26
AE24	VSS47	VSS126	AT28
AE26	VSS48	VSS127	AT30
AE27	VSS49	VSS128	AT32
AE29	VSS50	VSS129	AT34
AF31	VSS51	VSS130	AT39
AF38	VSS52	VSS131	AT42
AF4	VSS53	VSS132	AT46
AF42	VSS54	VSS133	AT7
AF46	VSS55	VSS134	AT74
AF5	VSS56	VSS135	ATJ30
AF7	VSS57	VSS136	AV16
AF8	VSS58	VSS137	AV20
AG19	VSS59	VSS138	AV24
AG2	VSS60	VSS139	AV30
AG31	VSS61	VSS140	AV38
AG48	VSS62	VSS141	AV43
AH11	VSS63	VSS142	AV8
AH3	VSS64	VSS143	AW14
AH36	VSS65	VSS144	AW18
AH40	VSS66	VSS145	AW2
AH42	VSS67	VSS146	AW22
AH46	VSS68	VSS147	AW26
AH7	VSS69	VSS148	AW28
AJ19	VSS70	VSS149	AW32
AJ21	VSS71	VSS150	AW34
AJ24	VSS72	VSS151	AW36
AJ33	VSS73	VSS152	AW40
AJ34	VSS74	VSS153	AW48
AK12	VSS75	VSS154	AV11
AK3	VSS76	VSS155	AY12
	VSS77	VSS156	AY22
	VSS78	VSS157	AY28
	VSS79	VSS158	

PANTHER-GP-NF

GP

<Core Design>

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Title		
PCH(9/9): GND		
Size	Document Number	Rev
A3	Colossus	1
Date: Monday, December 26, 2011		
Sheet 25 of 103		

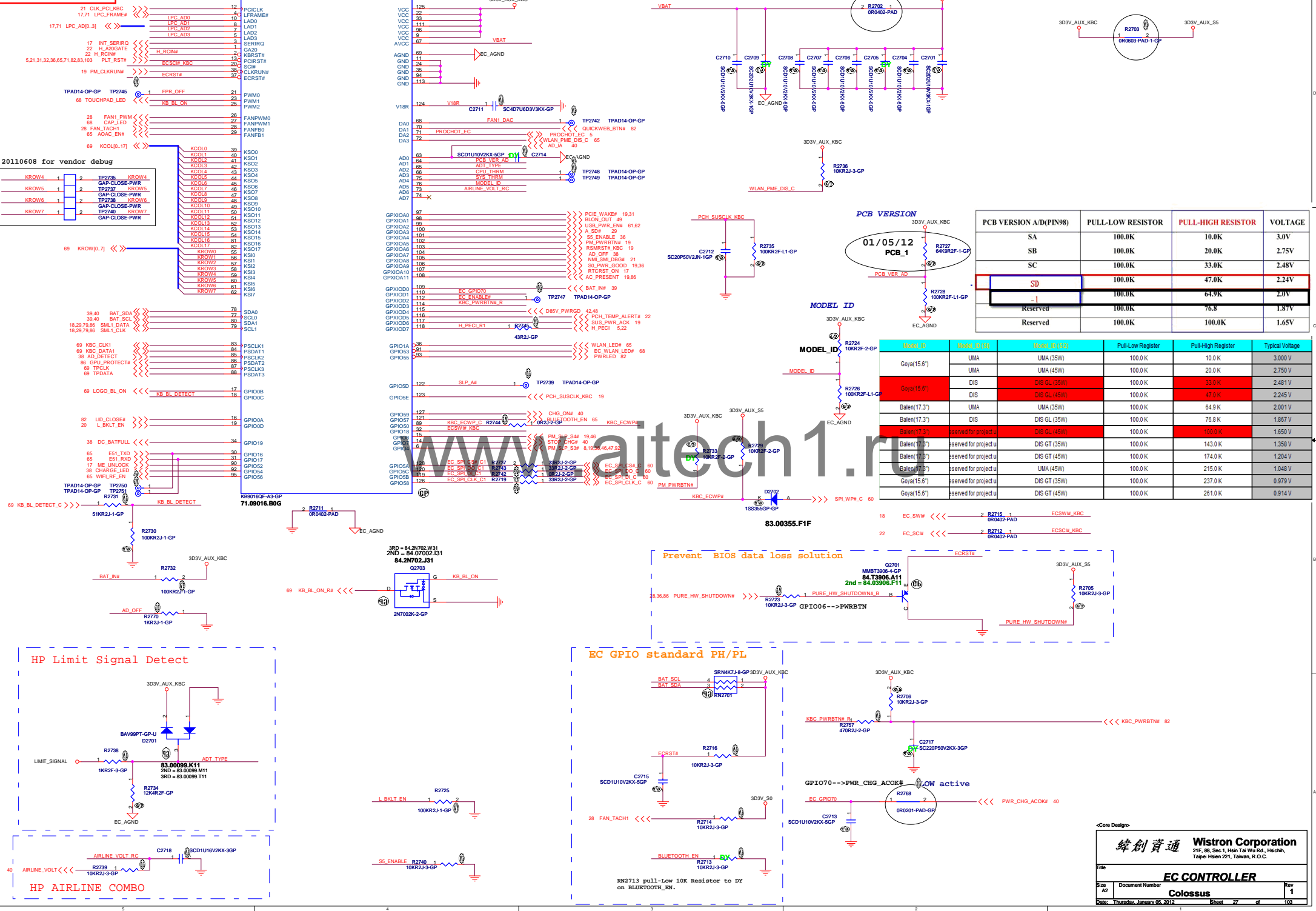
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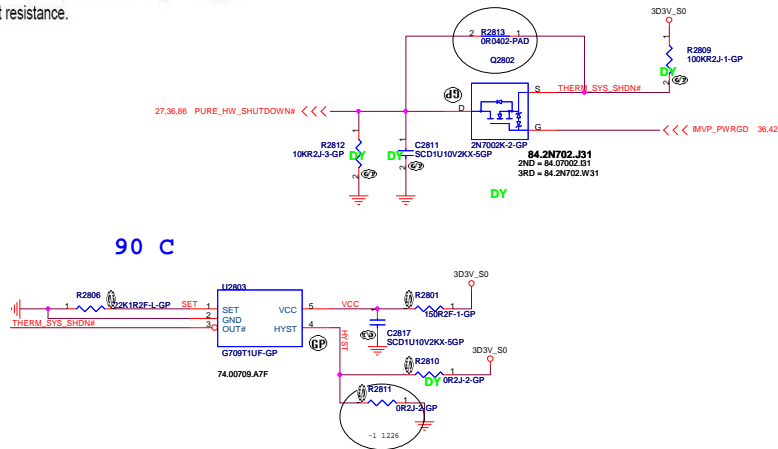
<div>緯創資通</div>		<div>Wistron Corporation</div>	
		<div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title			
<div>PCH XDP</div>			
Size	Document Number		Rev
A3	<div>Colossus</div>		1
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SSID = KBC



$$R_{SET}(k\Omega) = 0.0012T^2 - 0.9308T + 96.147$$

where T is the trip temperature in Centigrade. R_{SET} is the set-point resistance.



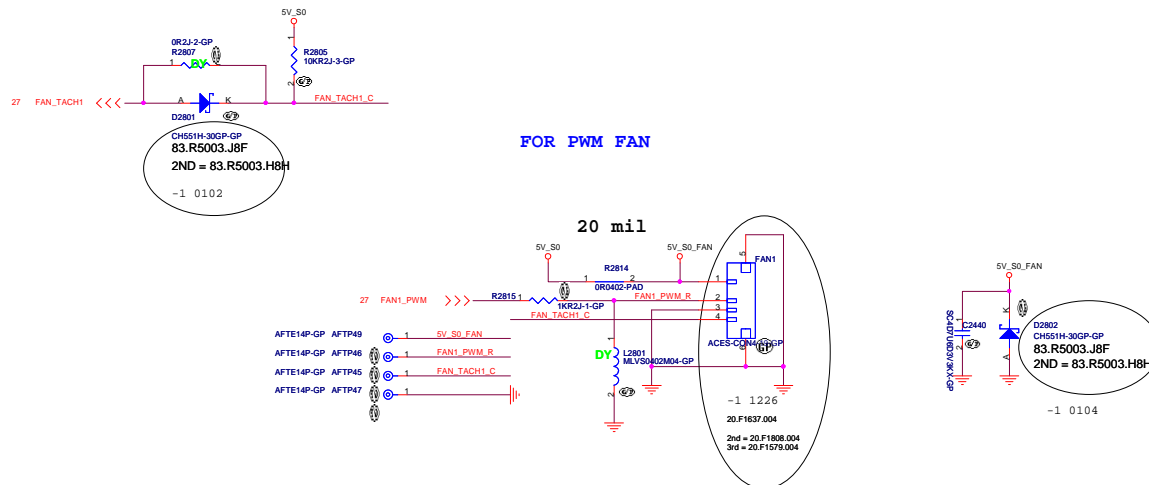
MT Global Mixed-mode Technology Inc.

G709/G710

Pin Description

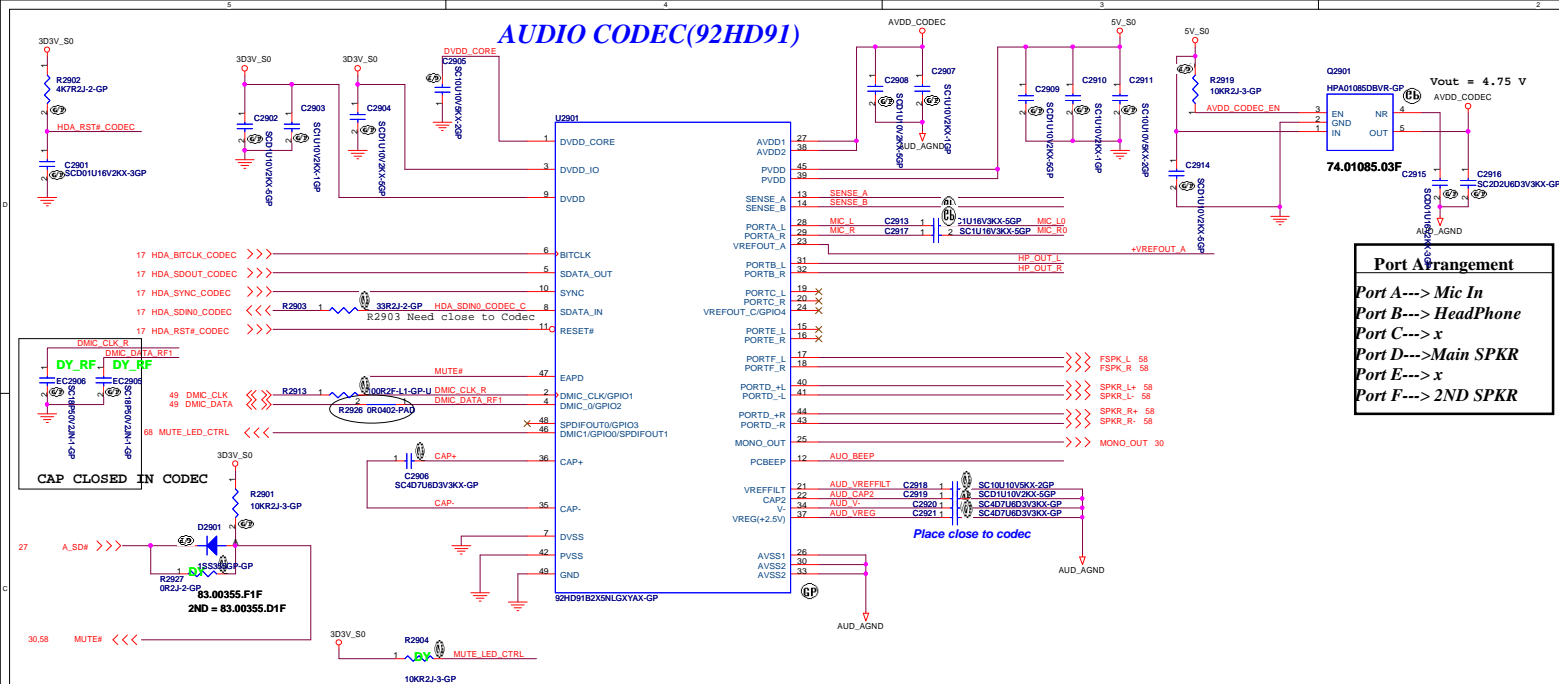
PIN	NAME	FUNCTION
G709	G710	
1	1	SET Temperature Set Point. Connect an external 1% resistor from SET to GND to set trip point.
2	2	GND Ground.
3	3	OT Open-Drain Active Low Output.
4	4	HYST Hysteresis Selection. Hysteresis is 10°C for HYST = V _{CC} , 2°C for HYST = GND.
5	5	N.C. Not Connected.
6	6	VCC Power-Supply Input.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
HYST Input Threshold	V _{IH}		0.7 x V _{CC}	---	---	V
	V _{IL}		---	---	0.3 x V _{CC}	V



<Core Design>

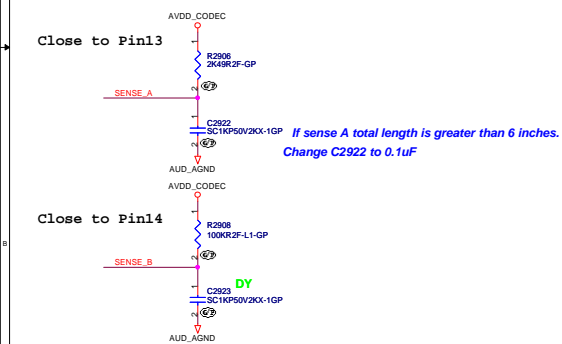
AUDIO CODEC(92HD91)



Port Arrangement

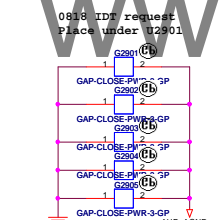
Port A--> Mic In
Port B--> HeadPhone
Port C--> x
Port D--> Main SPKR
Port E--> x
Port F--> 2ND SPKR

SENSE Detect Headphone Trace = 15mil



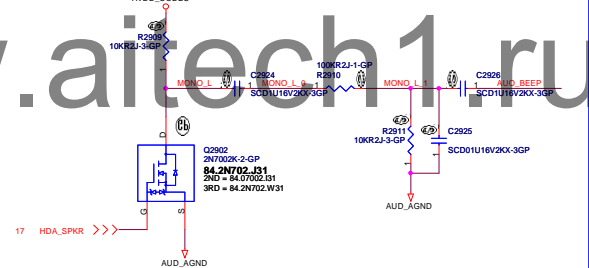
Digital GND & AUD_AGND

Tie Analog GND and Digital GND under codec by a single point

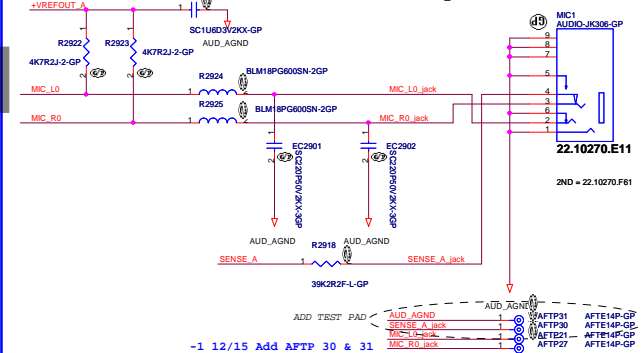


audio ground must be connect to digital ground with an 80 mil copper bridge located directly under codec to prevent ESD latch up.

PC BEEP

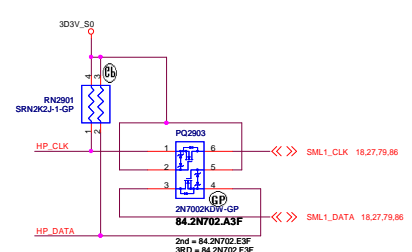
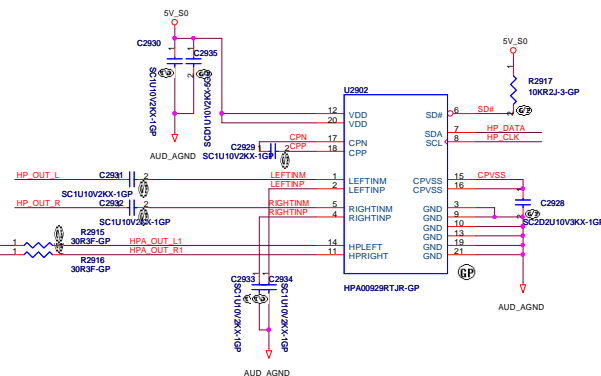
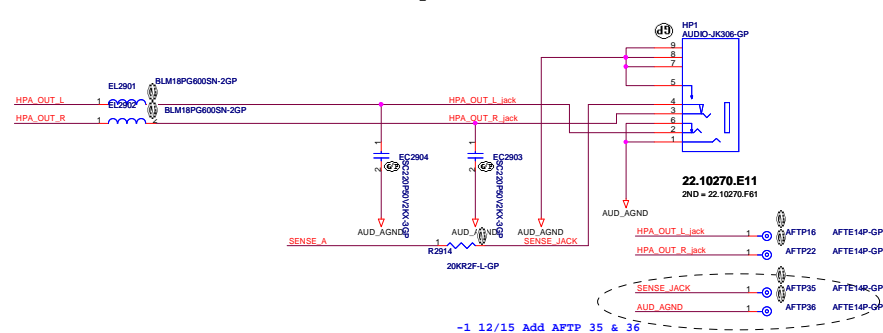


MIC IN ME update MIC1 Jack



HeadPhone

ME update HP1 Jack



◀Core Design▶

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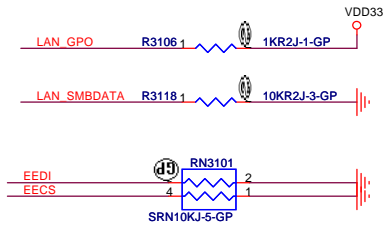
Title			
Audio Codec 92HD91/HeadphoneAMP			
Size	Document Number		Rev
A2	Colossus		1
Date:	Wednesday, January 04, 2012	Sheet 29 of	103

WOOFER
WOOFER
WOOFER

WOOFER
WOOFER
WOOFER

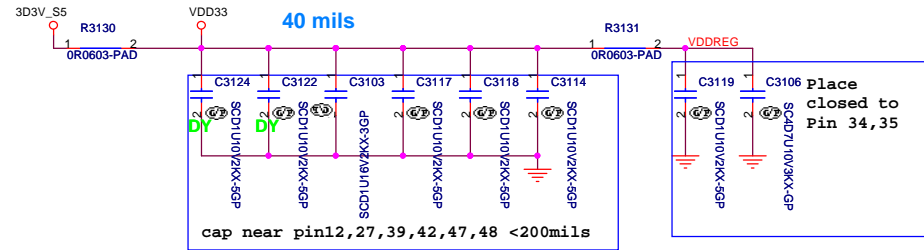


USE EFuse No ASF

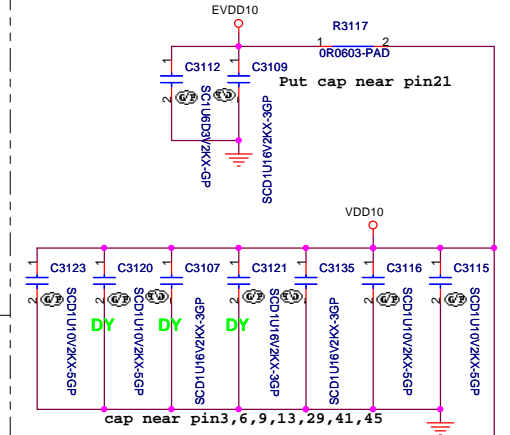


Avoid Leakage

LAN CHIP-RTL8111F

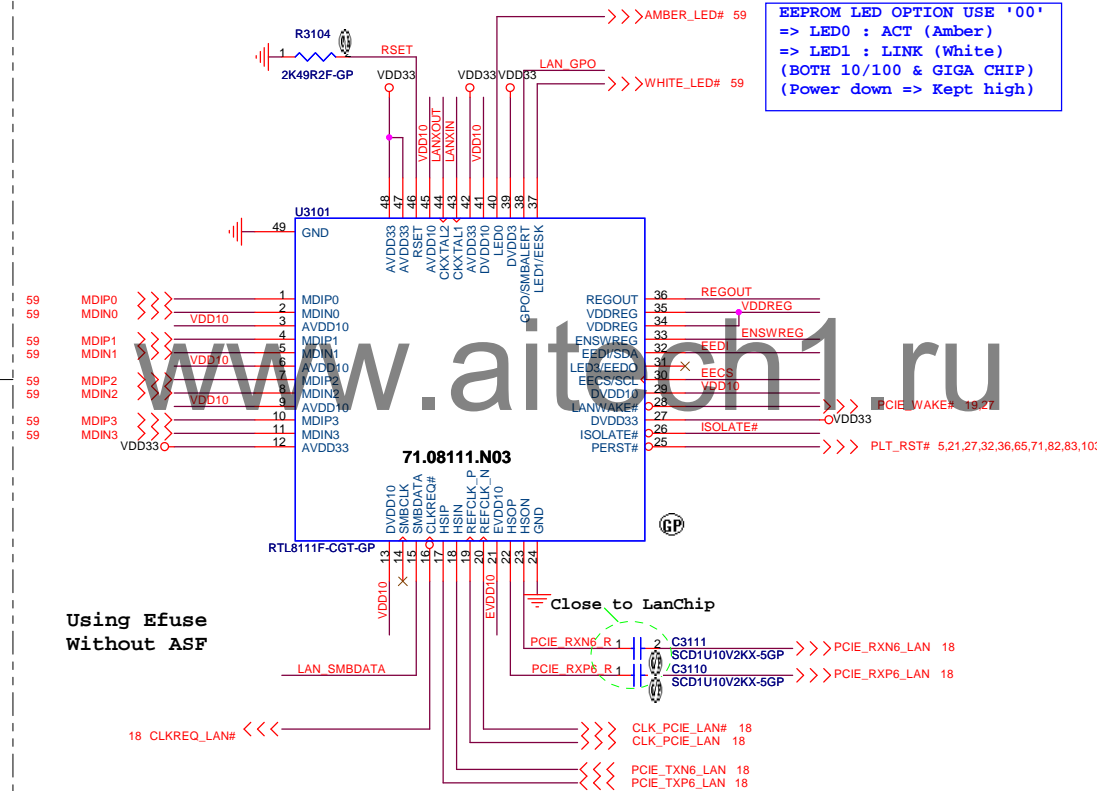


Regout power plane(1D05V)



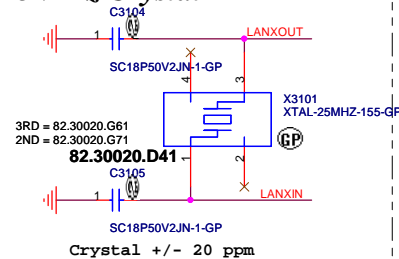
LanChip Power

+3.3V_LAN_S5 Rising time (10%~90%)
Spec >1ms and <100ms



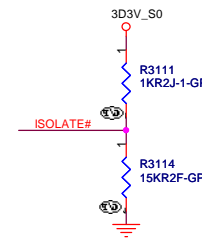
Using Efuse
Without ASF

25MHz Crystal

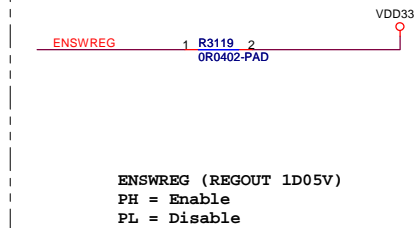


KBC Reserved Pin
Isolate# => Low , Isolate LanChip
GPO => EFuse Strap Pin

Isolate Strap Pin

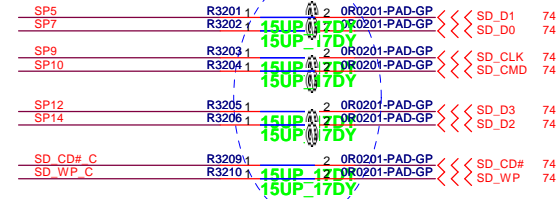


Regout Switch



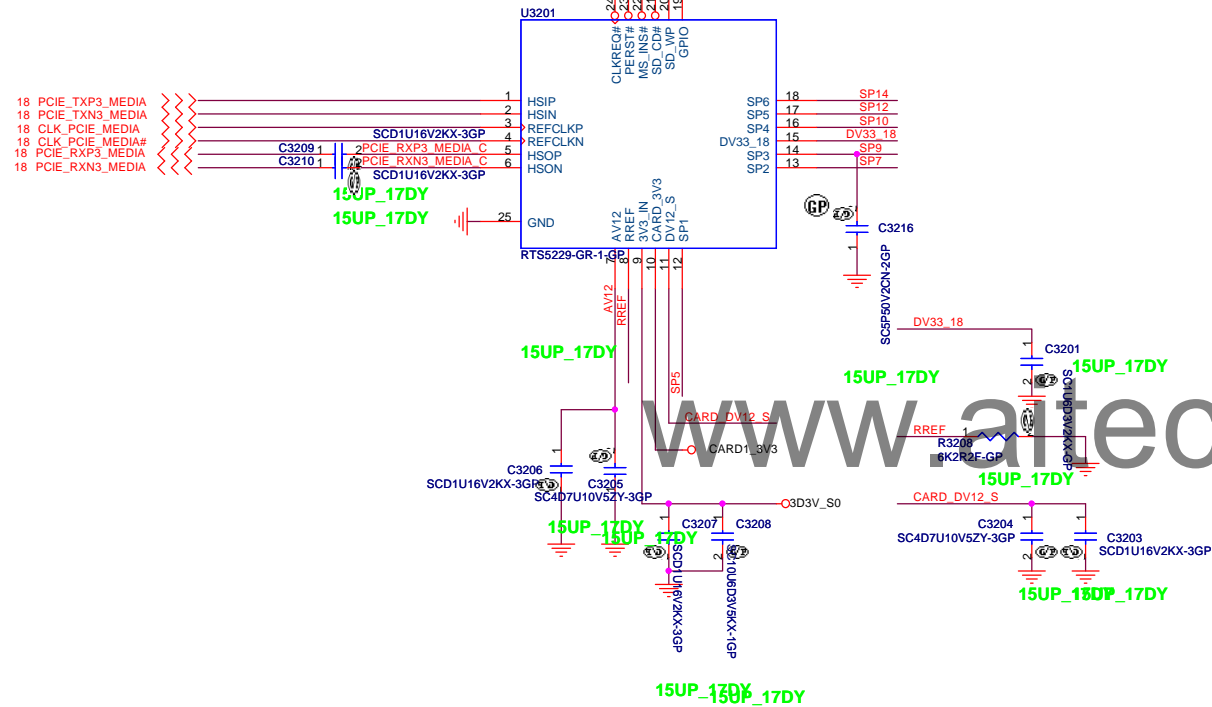
RTS5229

-1 12/15 0201 0 Ohm change to short pad



(RTS5229)U3201 closed near

Vendor info update design issue



www.altech1.ru

<Core Design>

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Card Reader-RTS5229			
Size A3	Document Number Colossus		Rev 1
Date: Wednesday, January 04, 2012		Sheet 32 of	103

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<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title1394

SizeA3

Document NumberColossus

Rev1

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size

A3

Document Number

Colossus

Rev

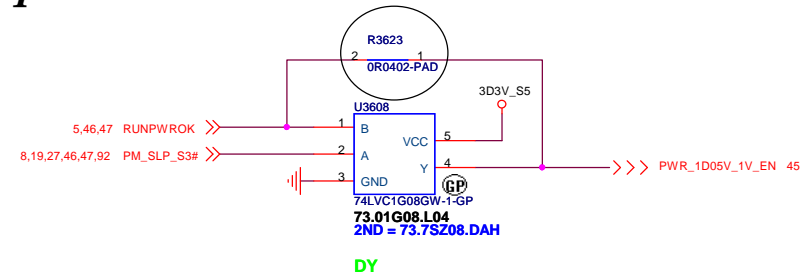
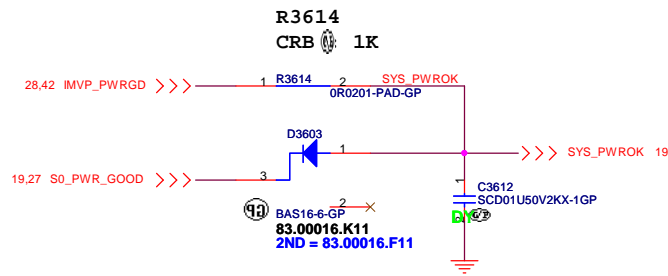
1

Date: Monday, December 26, 2011

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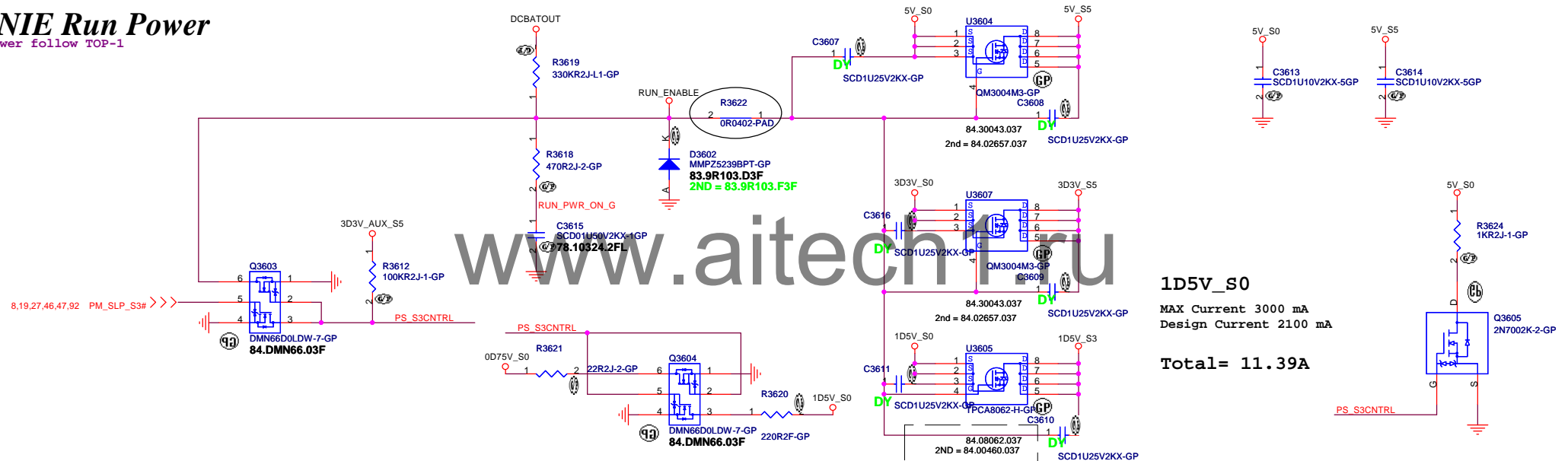
1

Power Sequence



ANNIE Run Power

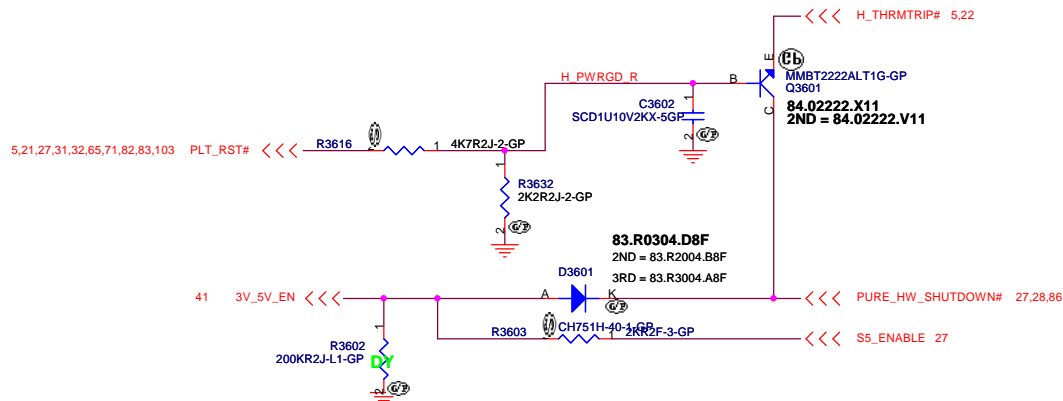
Run power follow TOP-1



1D5V_S0

MAX Current 3000 mA
Design Current 2100 mA

Total= 11.39A



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
Power Plane Enable			
Size A3	Document Number		Rev
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<Core Design>

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Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

Title

ADAPTER

Size
A3

Document Number
Colossus

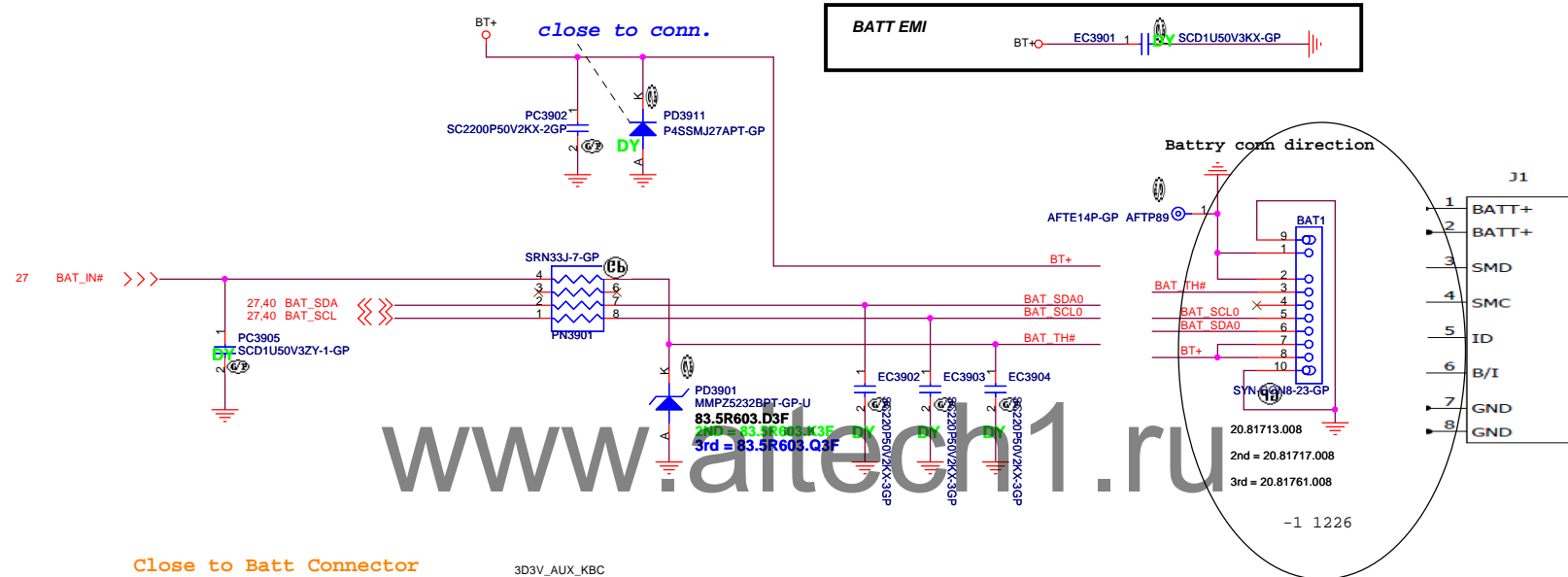
Rev
1

Date: Monday, December 26, 2011

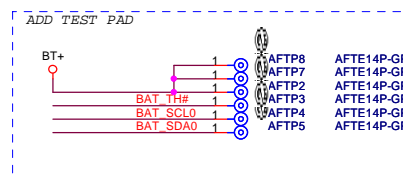
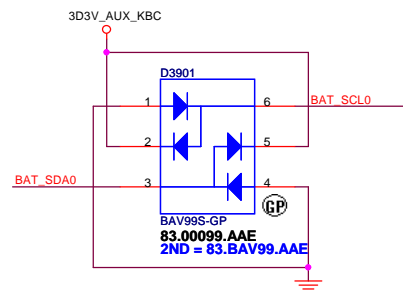
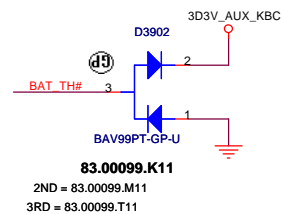
Sheet 37 of 103

1

BATT Connector



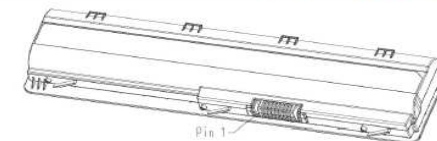
Close to Batt Connector



3. Interface

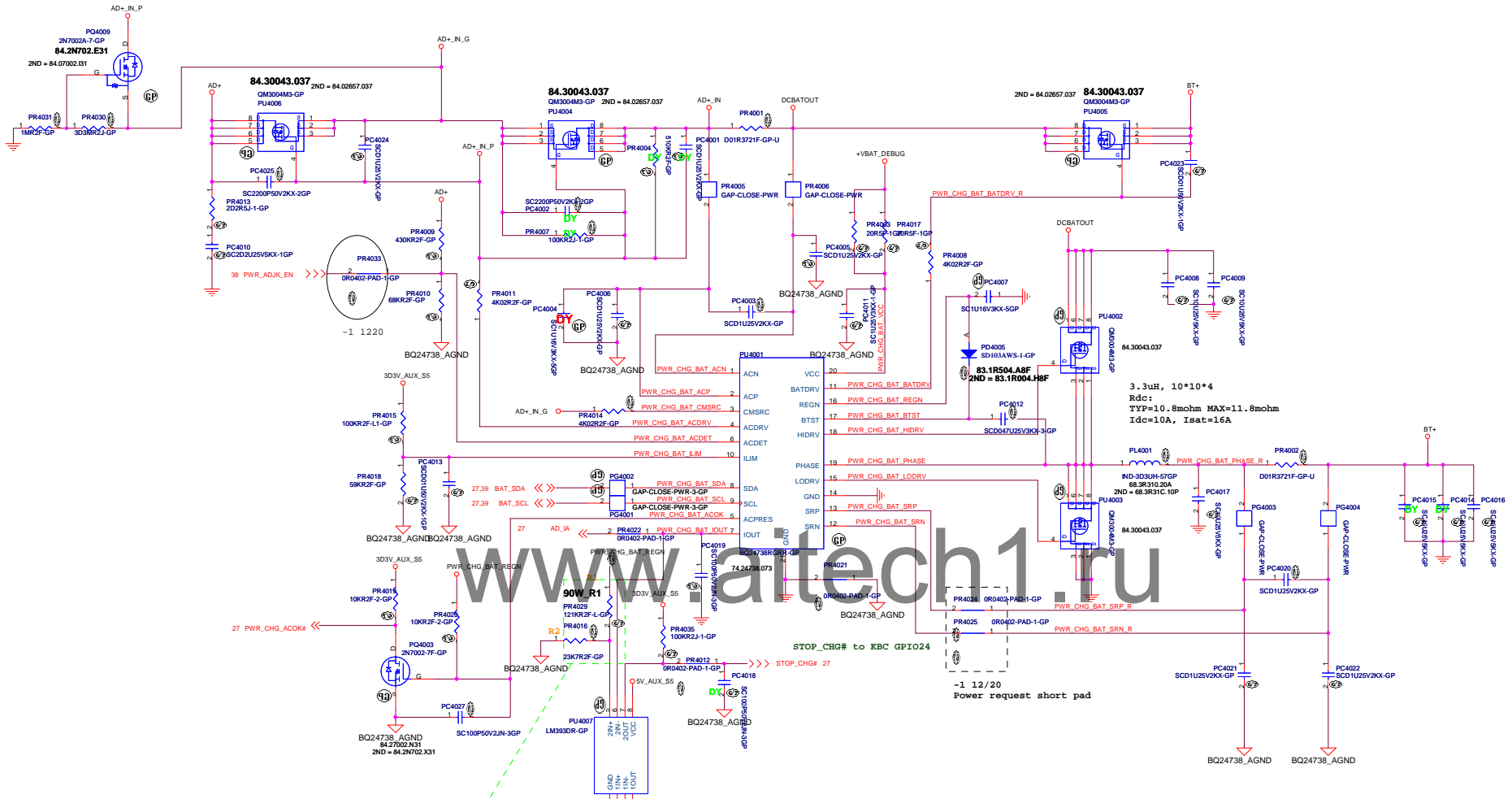
Connector ; 8pin
(Alltop C19029-10803-B, Foxconn BR0208C-B61H5-4H, Octek BTK-08ABEB)

Pin No.	Symbol	Description
1	BATT+	Batt+, Battery Positive Terminal
2	BATT+	Batt+, Battery Positive Terminal
3	SMD	SMBus data interface I/O pin
4	SMC	SMBus clock interface I/O pin
5	ID	Open
6	B/I	Connect to thermistor (103AT2 equivalent)
7	GND	Batt-, Battery Negative Terminal
8	GND	Batt-, Battery Negative Terminal

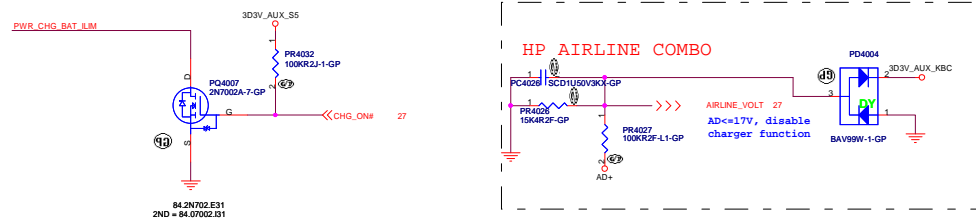


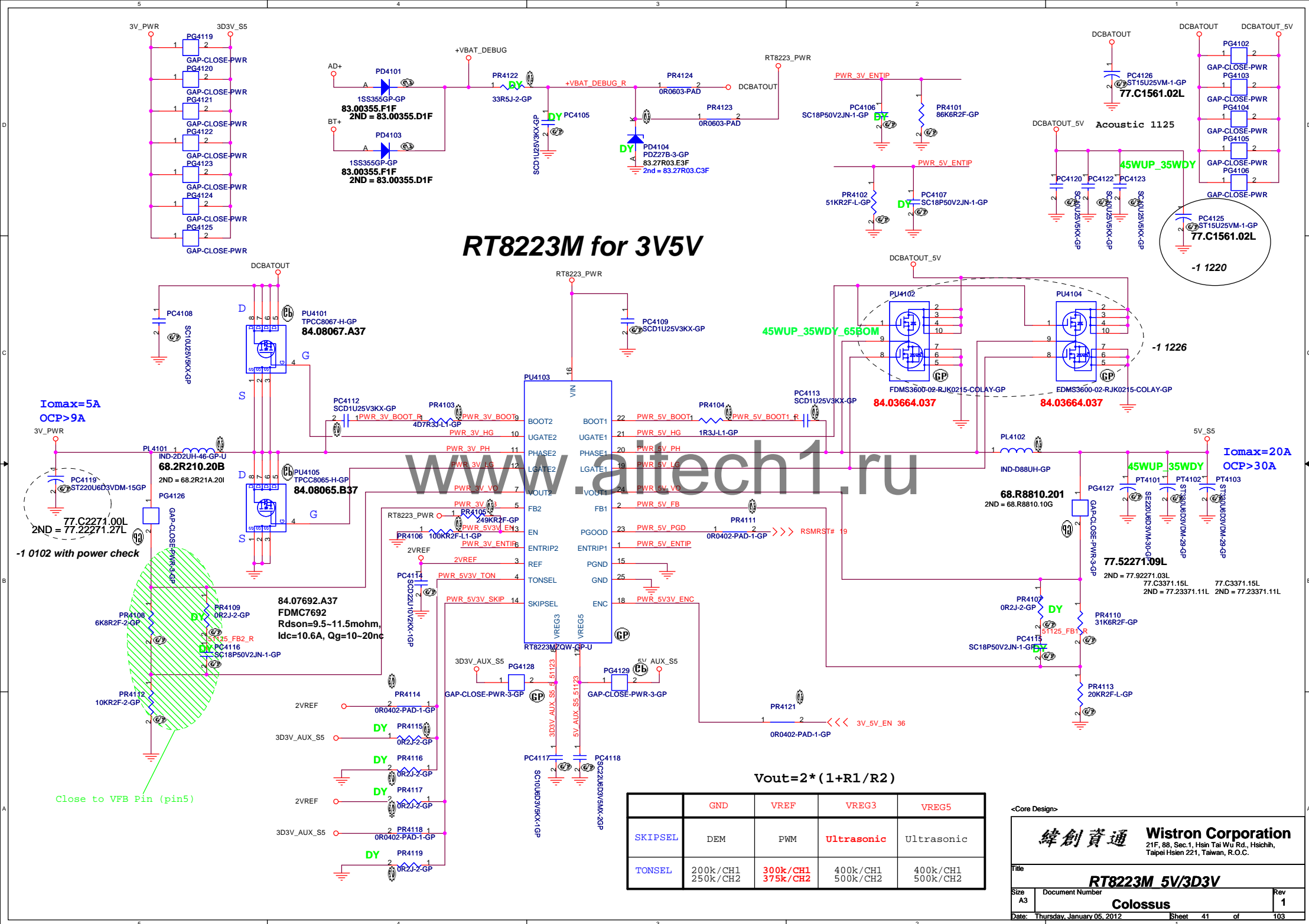
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title			
BATT CONN			
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AD+ total power	R1	R2
65W	178K	23.7K
90W	121K	23.7K
120W	84.5K	23.7K

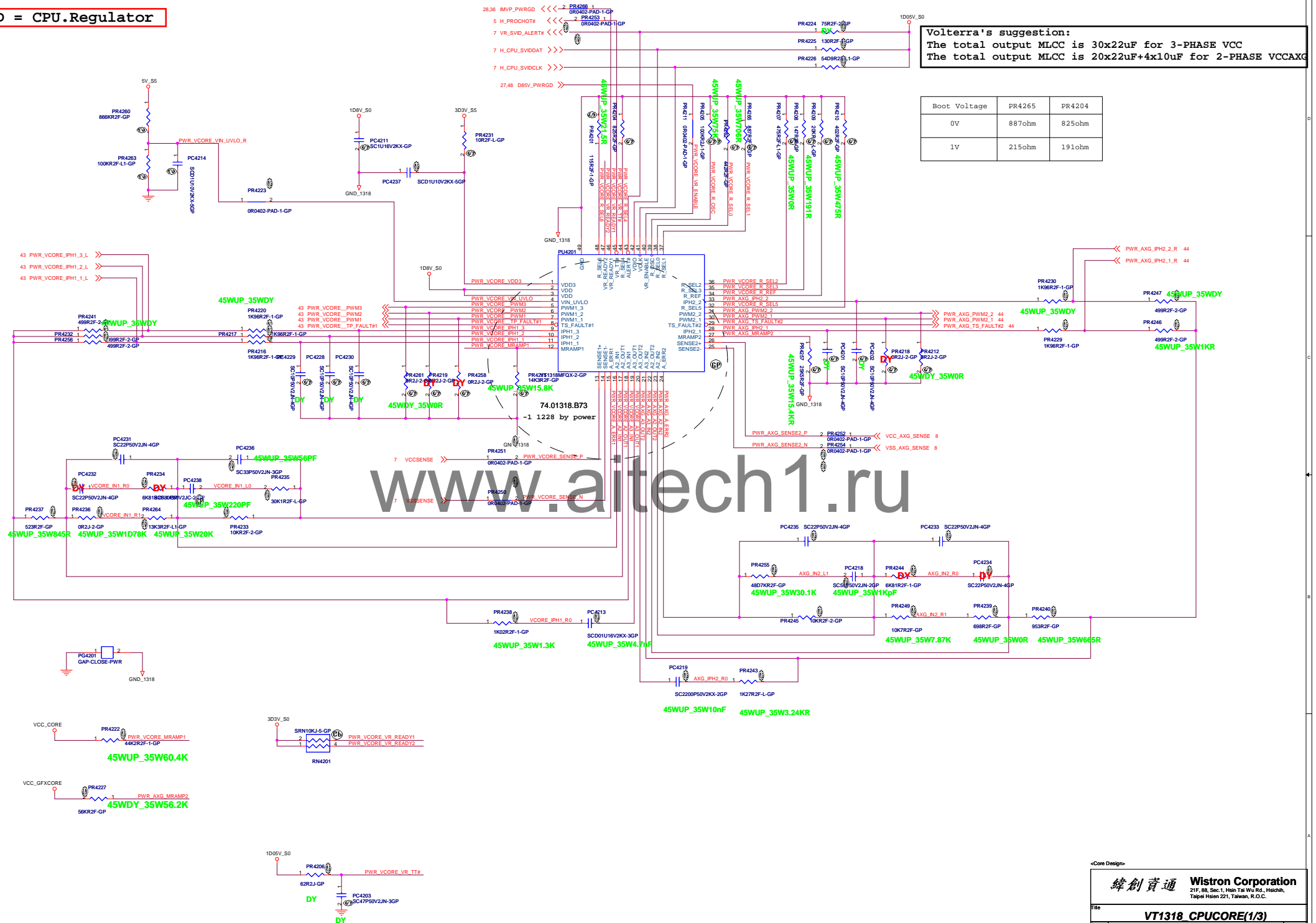





```
SSID = CPU.Regulator
```

<p>Volterra's suggestion:</p> <p>The total output MLCC is 30x22uF for 3-PHASE VCC</p> <p>The total output MLCC is 20x22uF+4x10uF for 2-PHASE VCCXG</p>
--

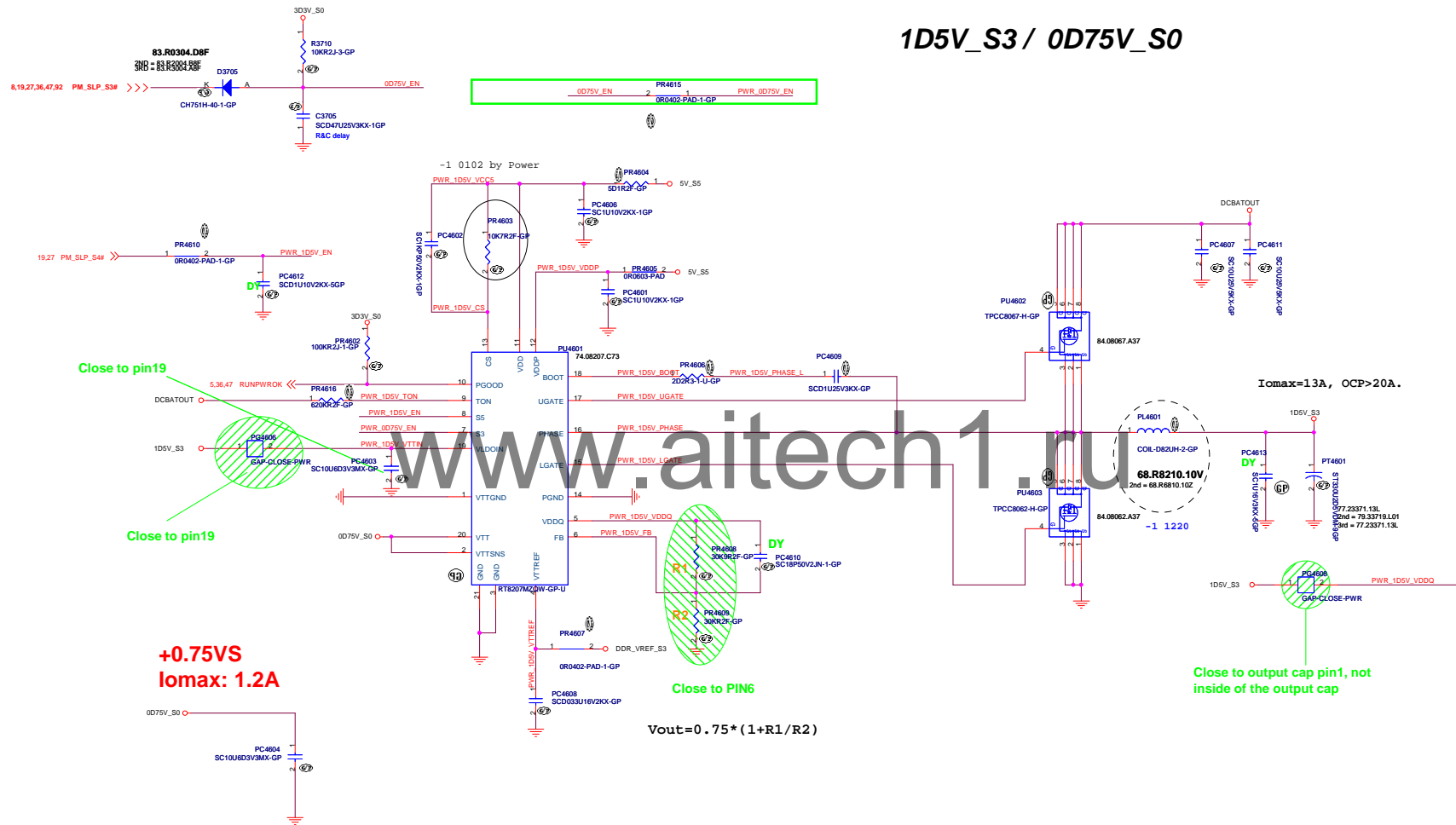
Boot Voltage	PR4265	PR4204
0V	887ohm	825ohm
1V	215ohm	191ohm






```
SSID = PWR.Plane.Regulator_1p5v0p75v
```

1D5V_S3 / 0D75V_S0



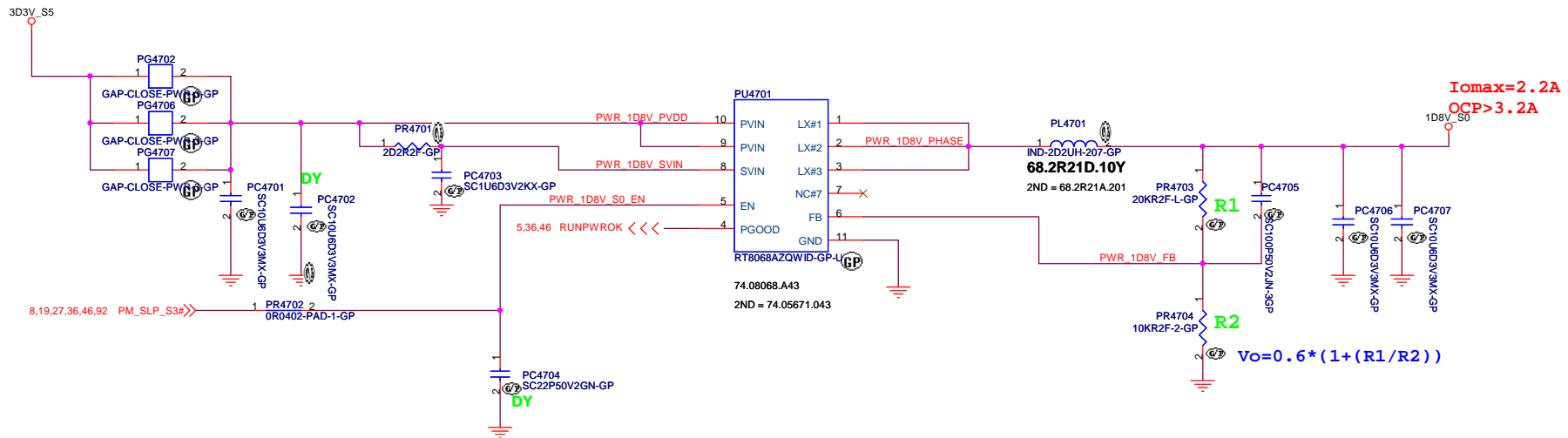
◀Core Design▶

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title			
RT8207MZ 1D5V & 0D75V			
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RT8068A for 1D8V_S0



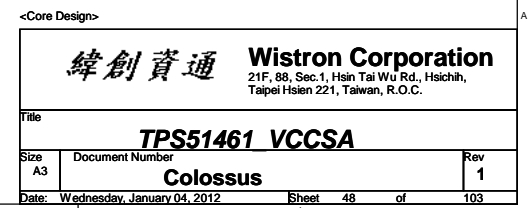
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<Core Design>

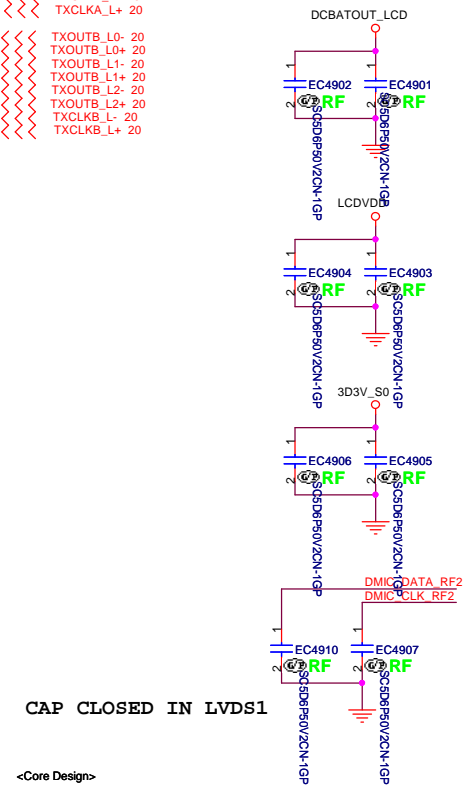
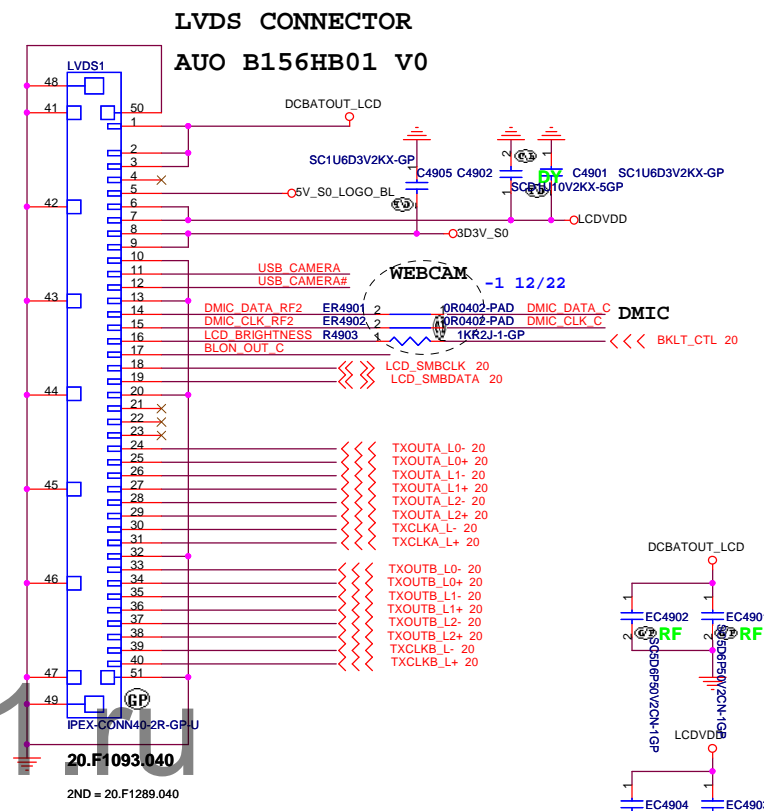
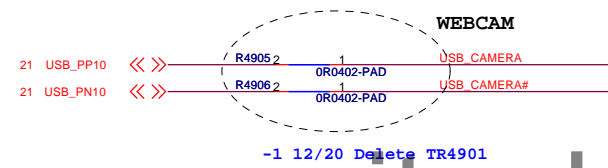
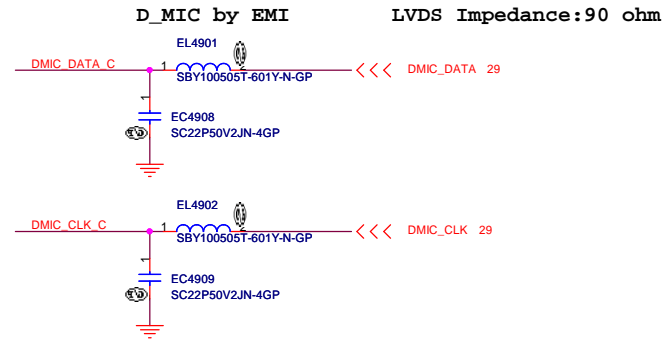
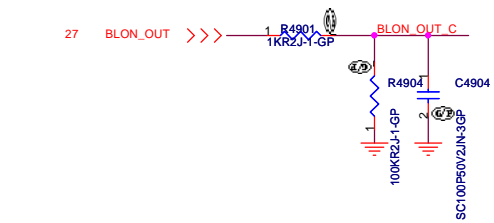
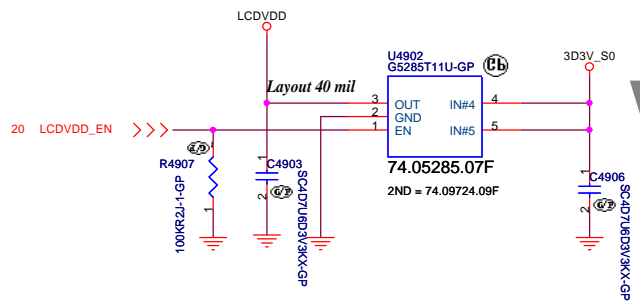
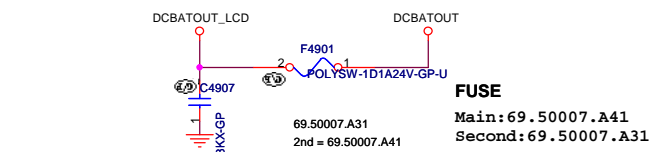
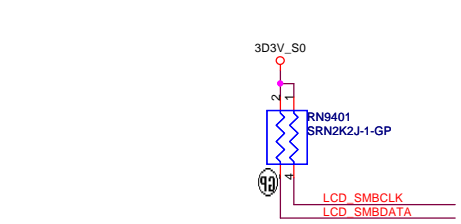
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title			RT8068A 1D8V	
Size	Document Number	Rev		
A3	Colossus	1		
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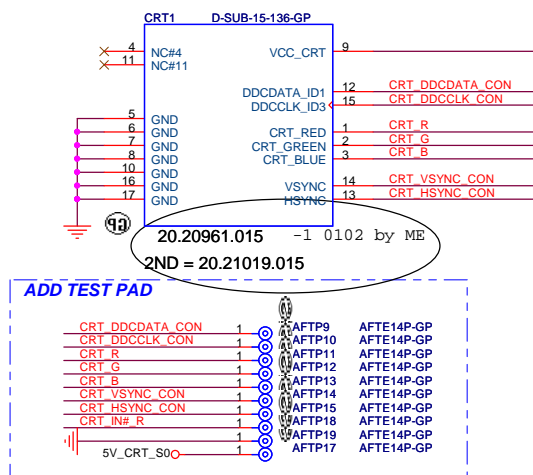
GND VREF COMP VOUT MODE
 TP551461RGER-GP
 74.51461.043
 0D85V_S0
 PR4811
 100R2F L1-GP-U
 COIL-D47UH-9-GP
 68.R4710.20G
 2ND = 68.R4710.20D



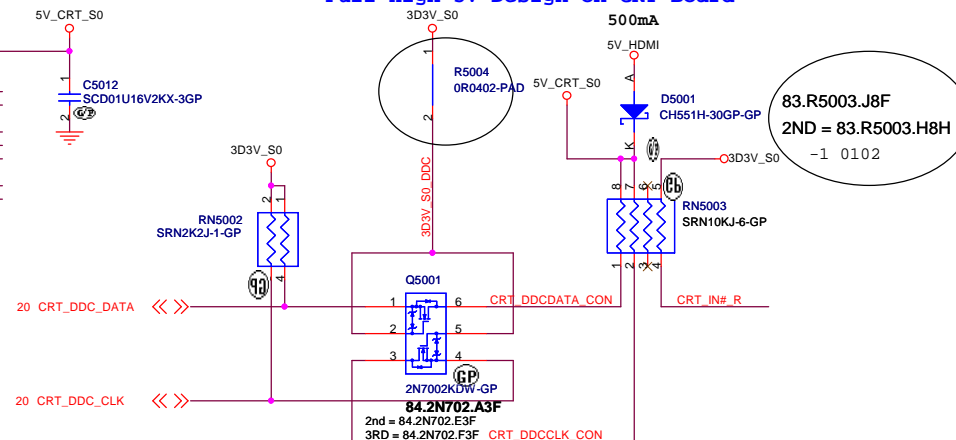
VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V



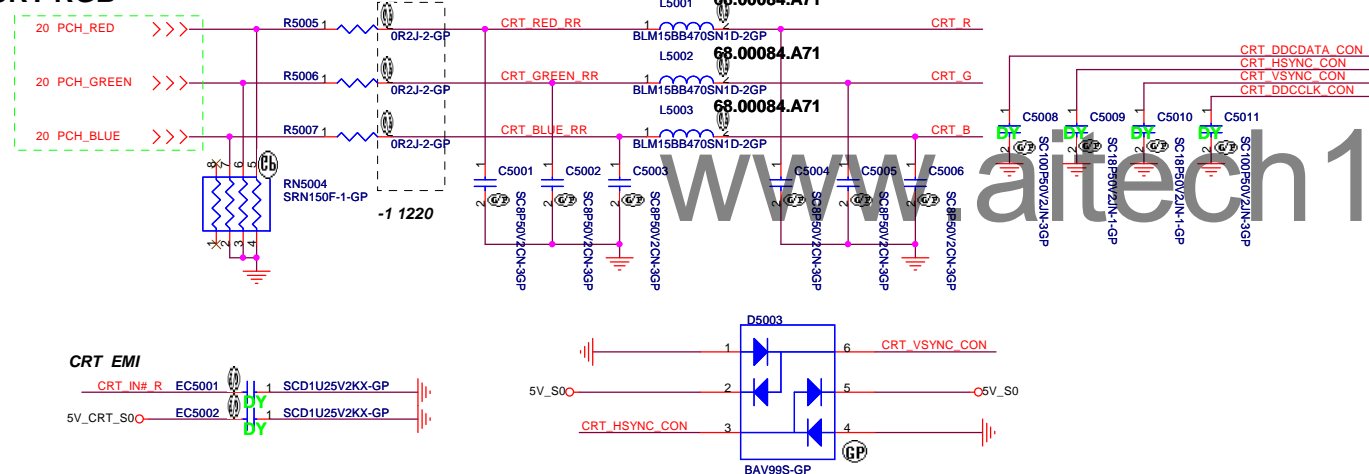
CRT Connector



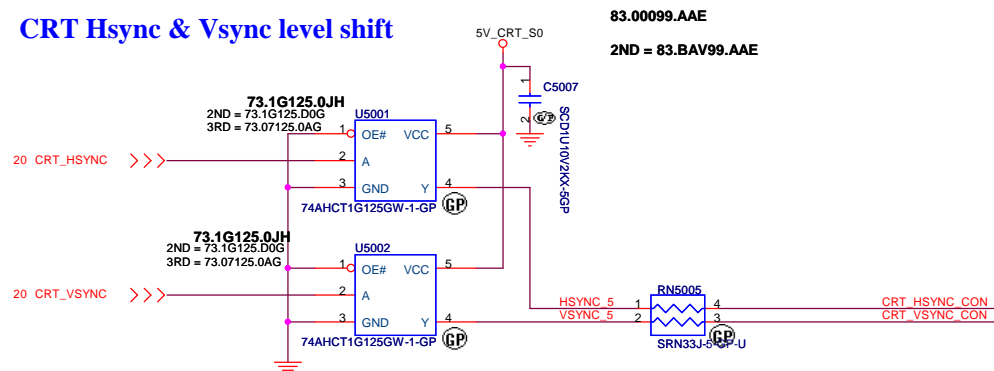
CRT DDCDATA & DDCCLK level shift



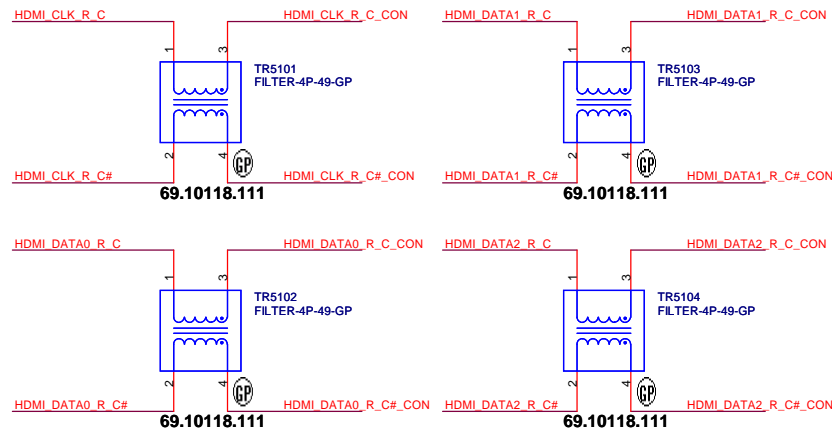
CRT RGB



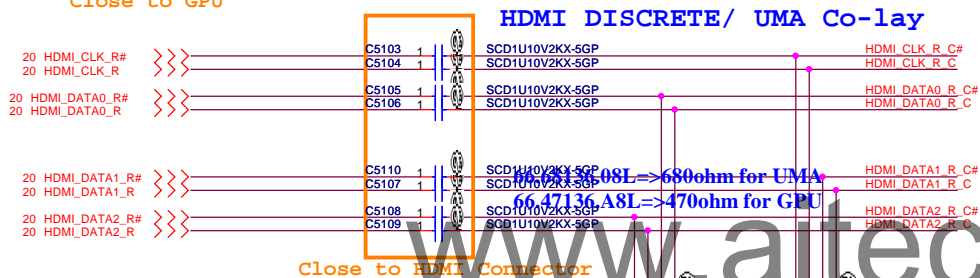
CRT Hsync & Vsync level shift



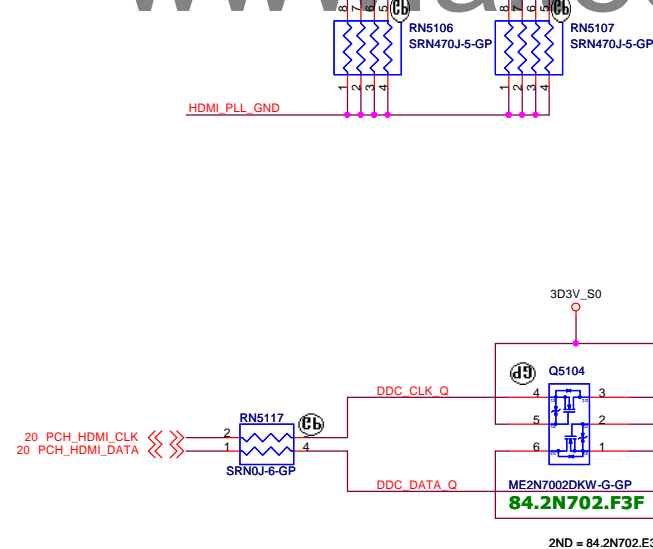
HDMI Level Shifter & CONNECTOR



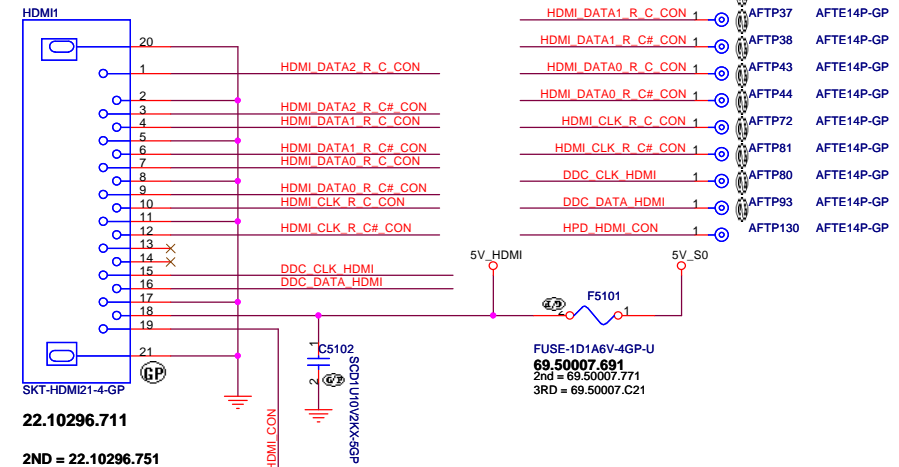
Close to GPU



Close to HDMI Connector

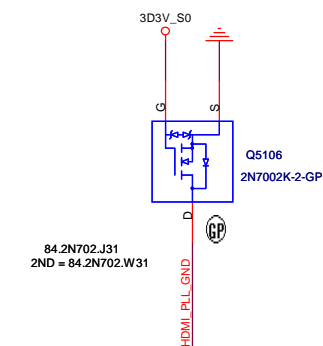
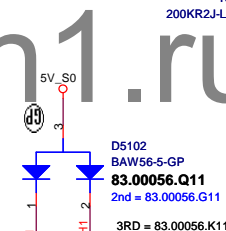


HDMI CONN



22.10296.711

2ND = 22.10296.751



Routing Guidelines:

CTRLDATA must be routed longer than CTRLCLK within 1000 mils (25.4 mm).
The total delay on CTRLDATA should be longer than CTRLCLK.

<Core Design>

(Blanking)

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<Core Design>

緯創資通

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Title

Display Port

Size
A3

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1

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<Core Design>

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Title

Reserved

Size
A3

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1

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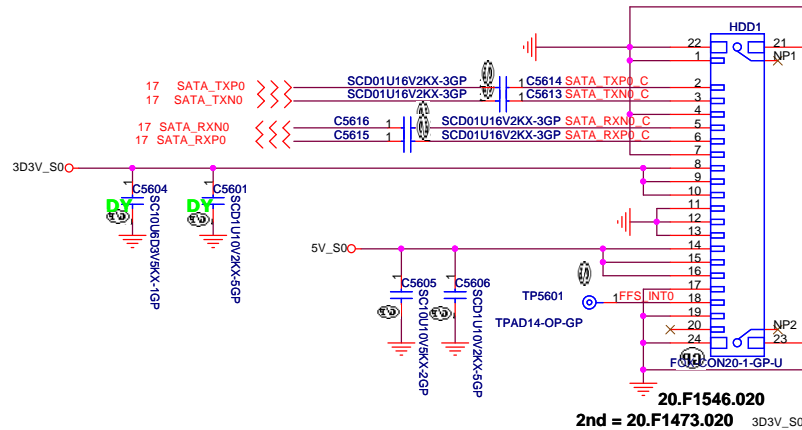
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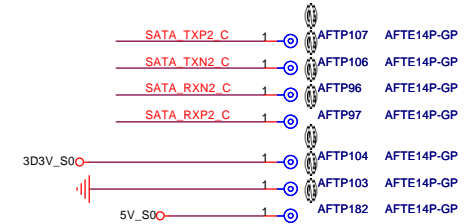
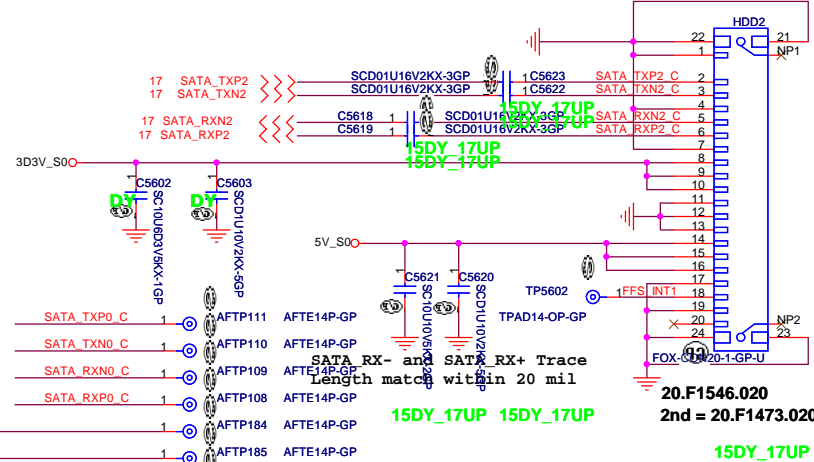
www.aitech1.ru

SATA HDD1 Connector

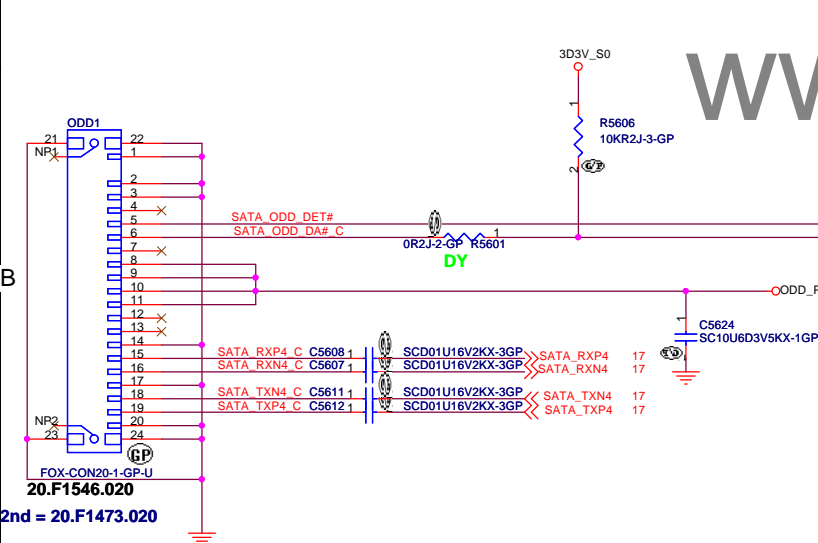
CHECK HDD conn model pin define_ME wire



SATA HDD2 Connector

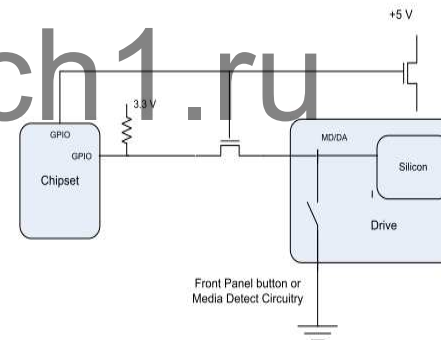


ODD Connector

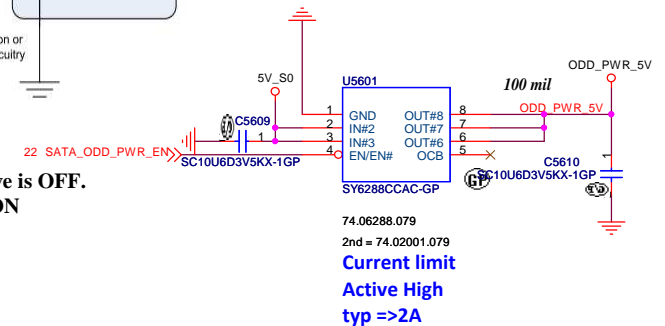


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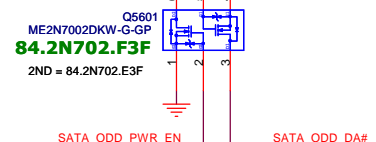
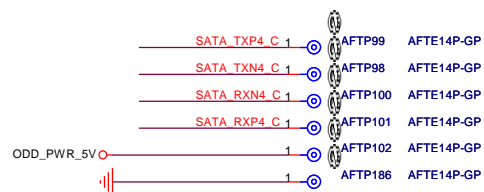
SATA Zero Power ODD



When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON



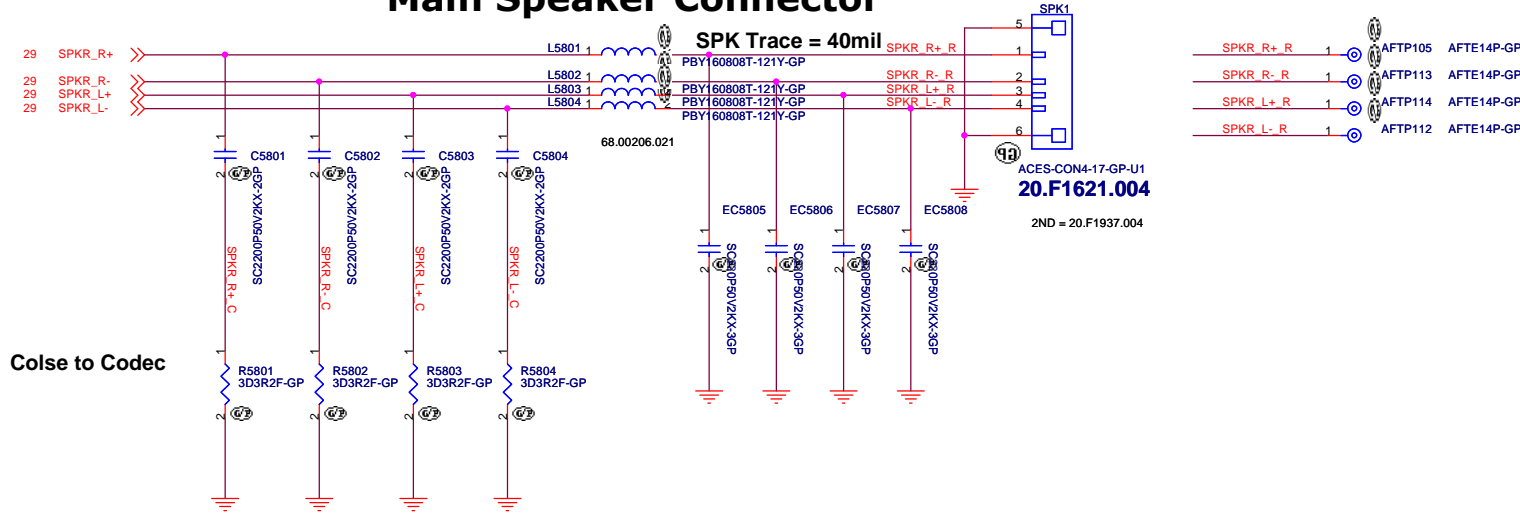
SUPPORT ZERO SATA ODD



(Blanking)

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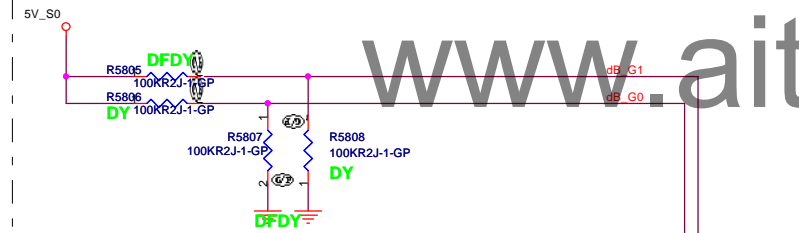
Main Speaker Connector



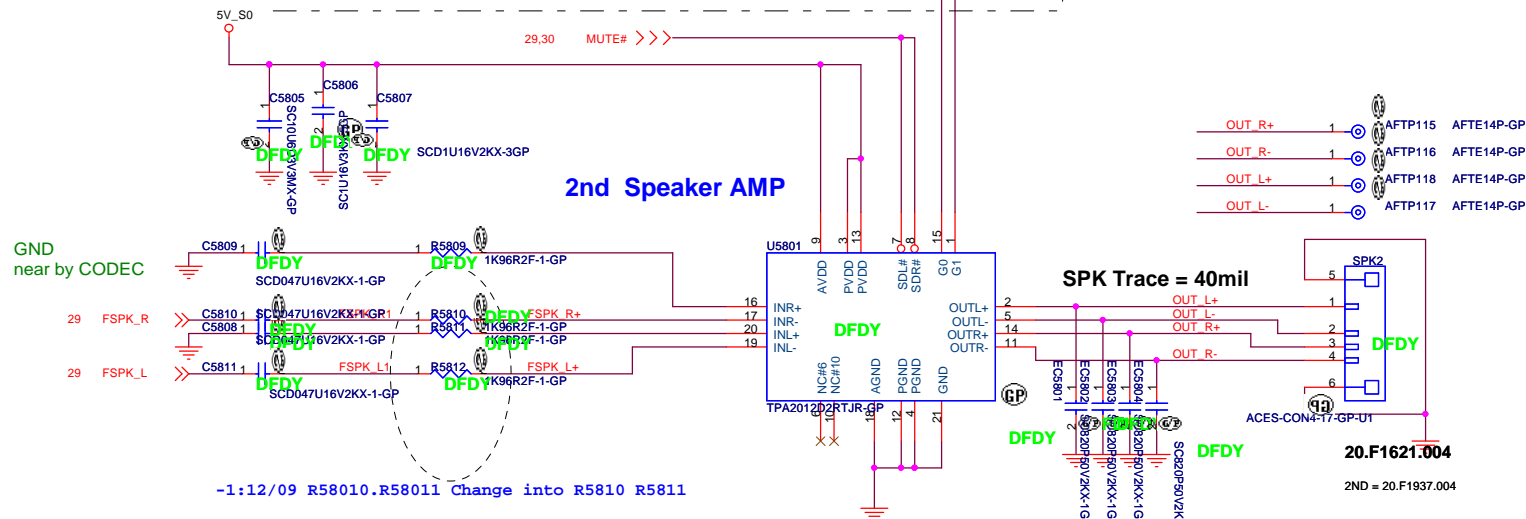
GAIN 18dB

G1	G0	V/V	Gain
0	0	2	6
0	1	4	12
1	0	8	18
1	1	16	24

2ND Speaker Connector



2nd Speaker AMP



<Core Design>

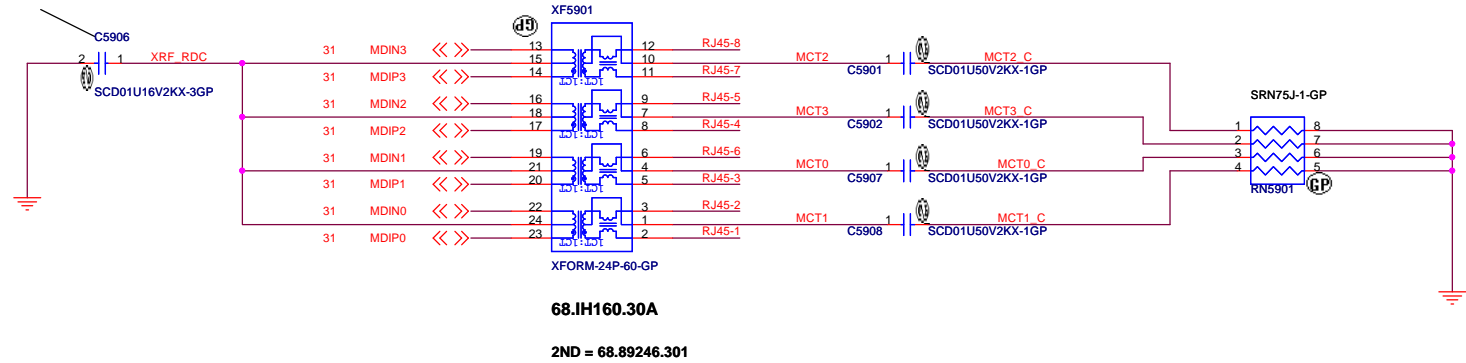
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
SPEAKER CONN		
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White LED for connectivity and Amber LED for activity located on RJ-45 connector

close to XF1

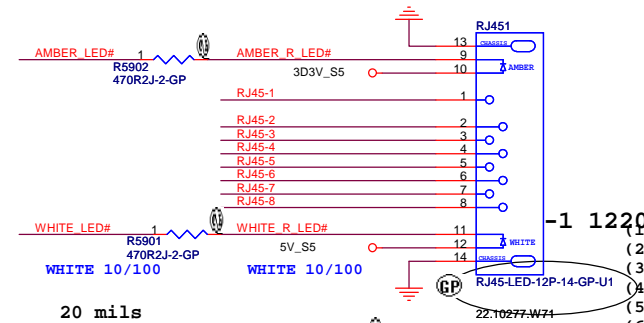
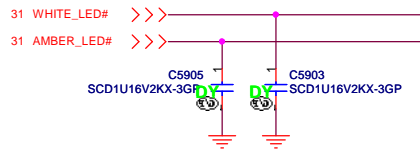
close to XF1



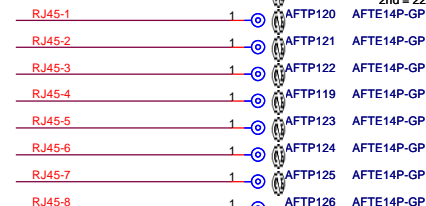
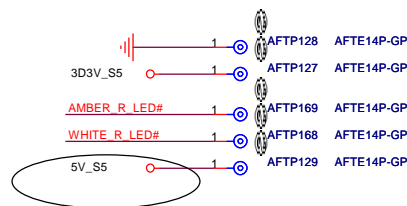
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AMBER = LAN ACK

RJ451



- 1 1220
- (1) route on bottom as differential pairs.
 - (2) Tx+/Tx- are pairs. Rx+/Rx- are pairs.
 - (3) No vias, No 90 degree bends.
 - (4) pairs must be equal lengths.
 - (5) 6mil trace width, 12mil separation.
 - (6) 36mil between pairs and any other trace.
 - (7) Must not cross ground moat, except RJ-45 moat.

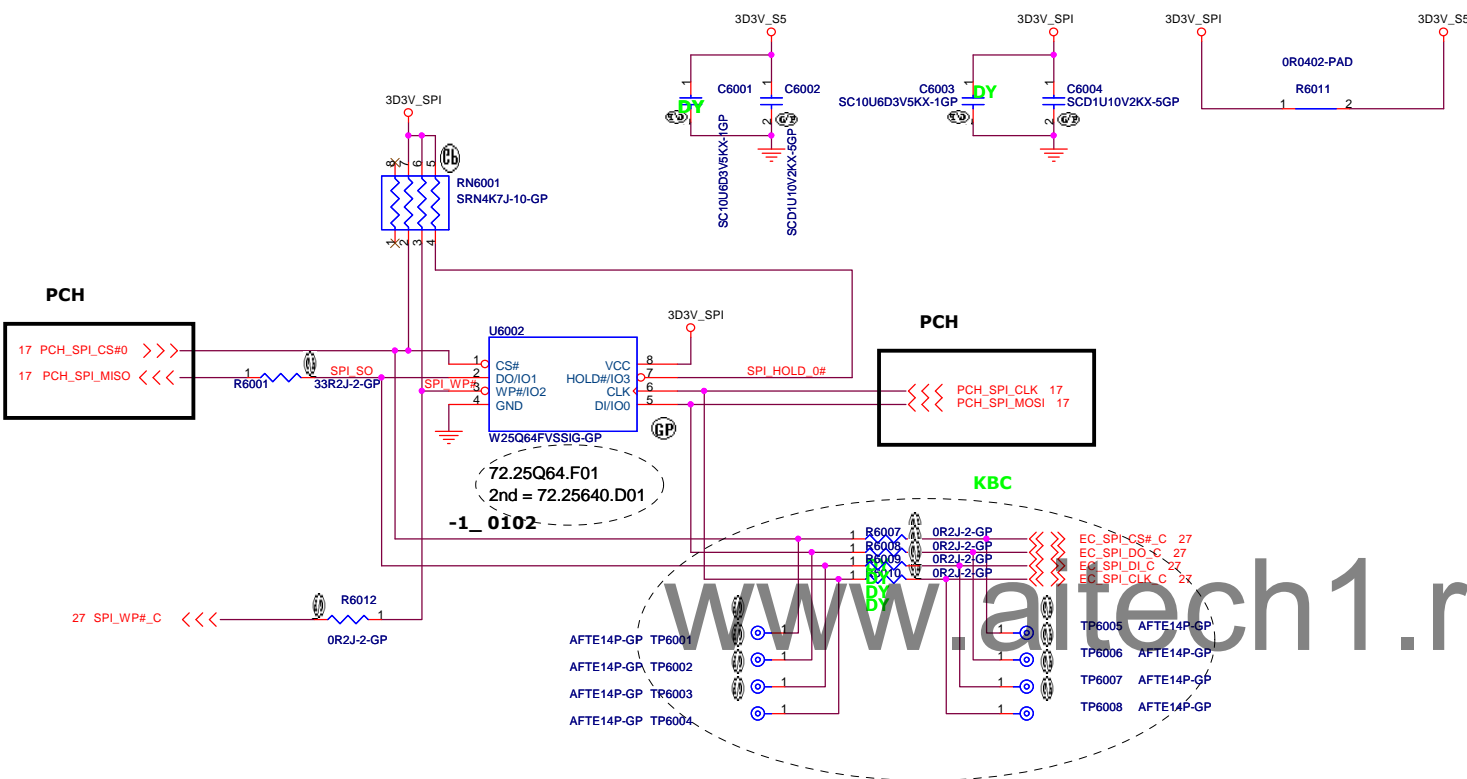


<Core Design>

緯創資通 Wistron Corporation
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SPI FLASH ROM (8M byte) for PCH & KBC

The total SPI interface signal between EC and PCH can't not exceed 6500mil. The mismatch between SPI signal must be within 500mil

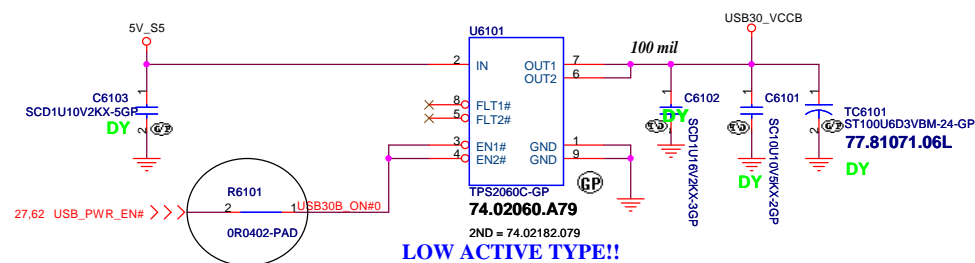


-1 1223 Reversed TP6001~TP6008 / R6007~R6010 is DY
1, 測試點請使用14mil, 測試之間距離75mil以上。
2, 測試點必須在Top層。

RESERVED USB 2.0/3.0 BD

SSID = USB

Power switcher Low active



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<Core Design>

緯創資通

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Title

USB Power SW USB IO

Size
A3

Document Number

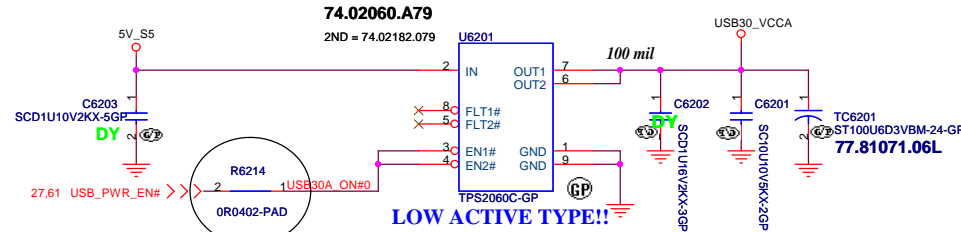
Colossus

Rev
1

Date: Wednesday, January 04, 2012

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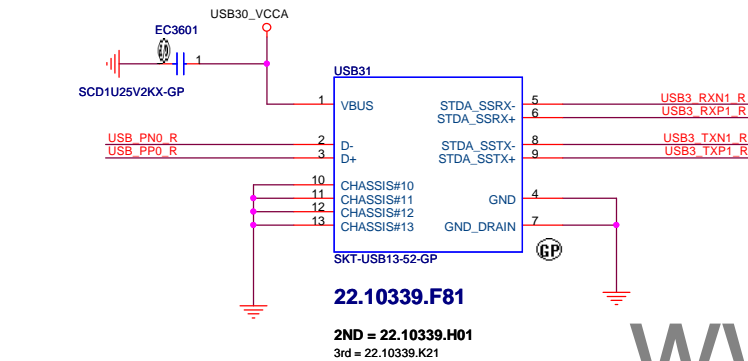
Power switcher Low active



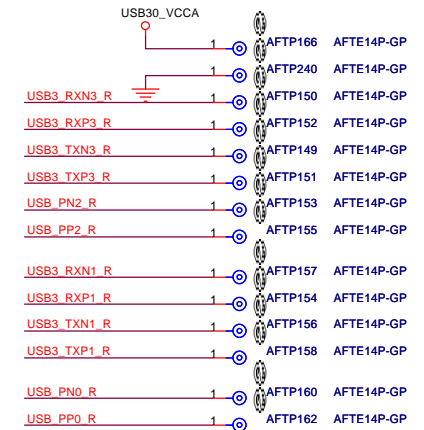
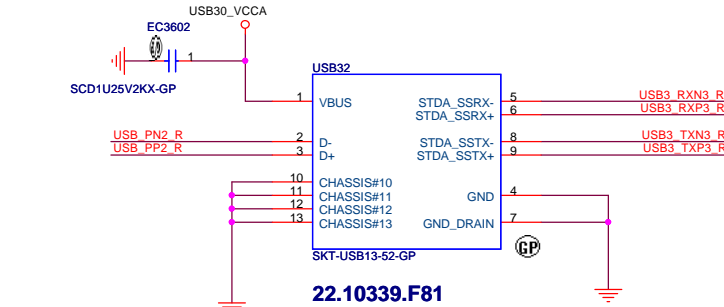
USB 3.0 Connector Pin definition

Pin	Signal
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+ SuperSpeed RX
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+ SuperSpeed TX

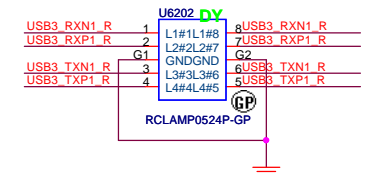
USB3_1



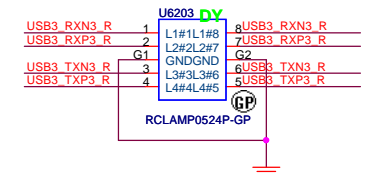
USB3_2



Ultra Low Capacitance TVS Arrays (Pin5.6.7.8 No Internal Connection)



Ultra Low Capacitance TVS Arrays (Pin5.6.7.8 No Internal Connection)



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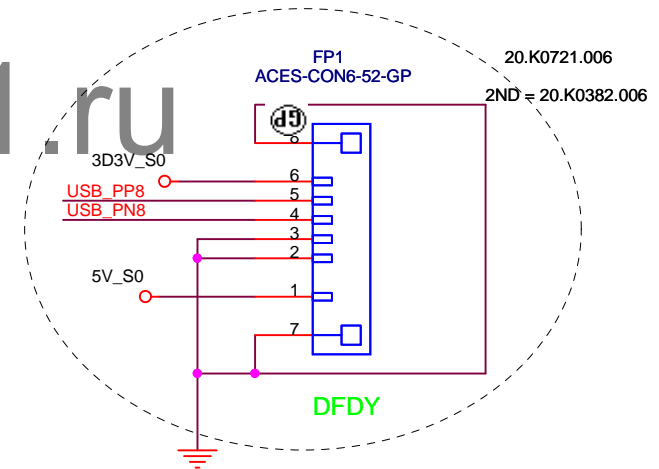
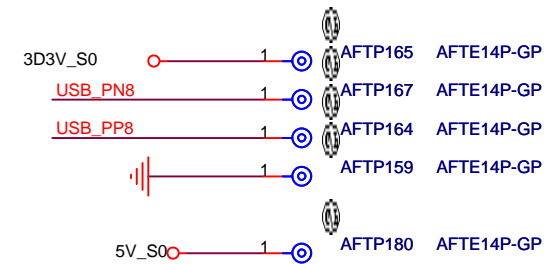
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Title		
USB3.0		
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Date:	Thursday, January 05, 2012	Sheet 62 of 103

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<Variant Name>			
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Resered(Bluetooth)			
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-1 12/23 FP1 change source

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Finger Print Conn

Rev

1

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SSID = Wireless

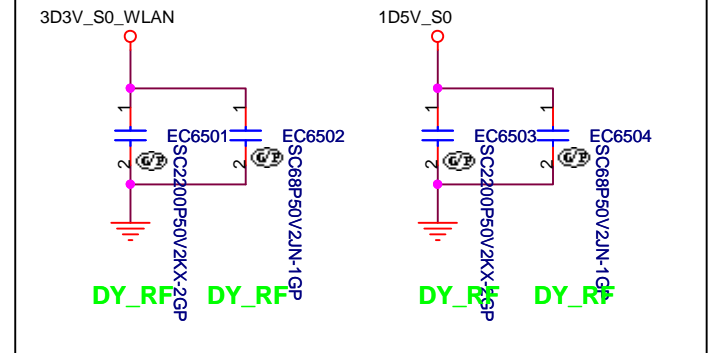
Mini-Card--WLAN

Half minicard

Mini-Card--WLAN

Half minicard

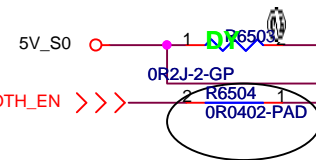
CLOSED IN WLAN1



51 BT_DISABLE_L
(low active to disable Bluetooth)

Pin	Active	Function
5	High(3V)	GPIO/BT_WAKE
20	High(3V)	WIFI_Enable
47	Reserved	BT_PRISEL(coexistence)
51	Reserved	BTCX_STAT(coexistence)

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2ND = 20.F1697.052
3RD = Main:62.10043.F91

677869-FM8

1st	677869-FM8
2nd	677869-AM8
3rd	677869-BM8
4th	677869-LM8

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title MINICARD(WLAN+Bluetooth)/CONN	
Size A4	Document Number Colossus
Date Wednesday, January 04, 2012	Rev 1
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Title

Reserved

Size
A3

Document Number
Colossus

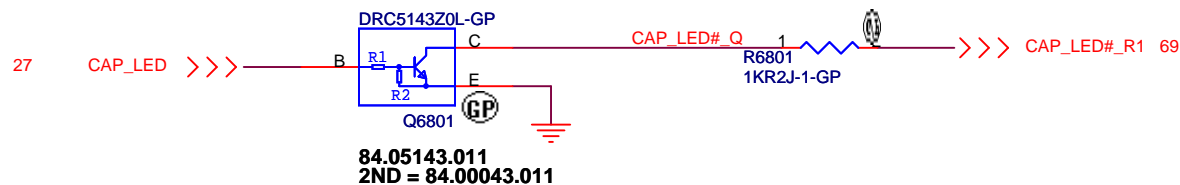
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1

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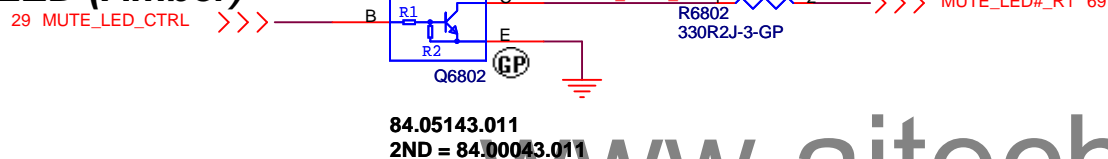
SSID = User.Interface

On Keyboard LEDs

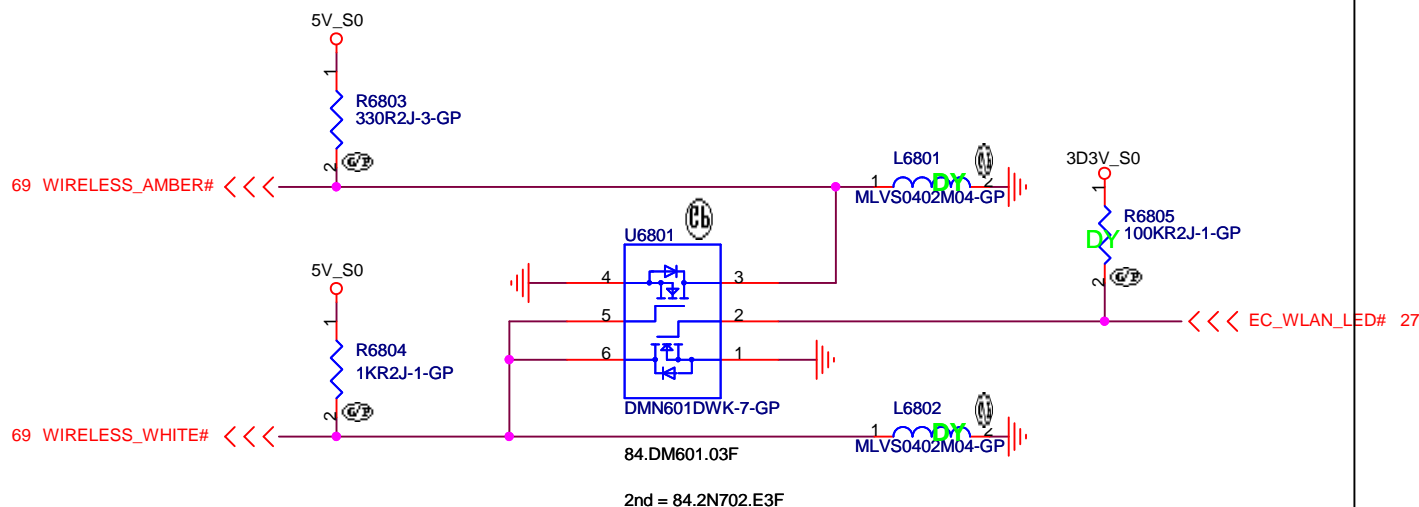
Cap locks LED (White)



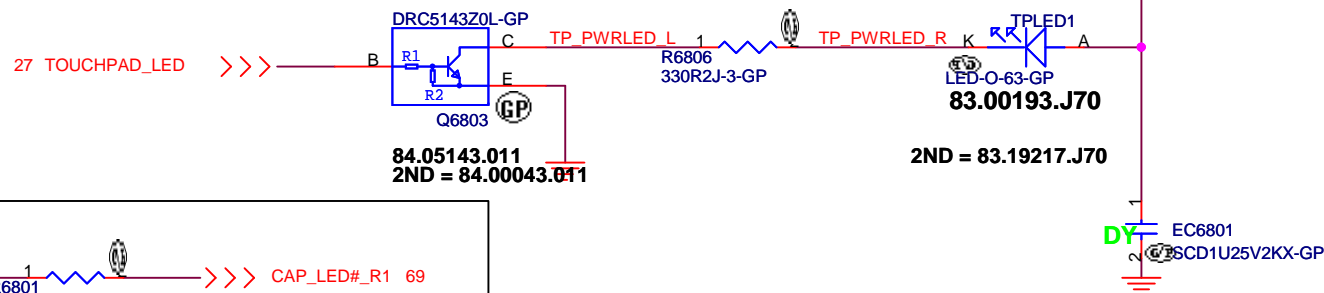
Mute LED (Amber)



Wireless LED (White-On, Amber-Off)



Touchpad LED (Amber)



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Title

LED Bard/Power Button

Size
A4

Document Number

Colossus

Rev

1

Date: Wednesday, January 04, 2012

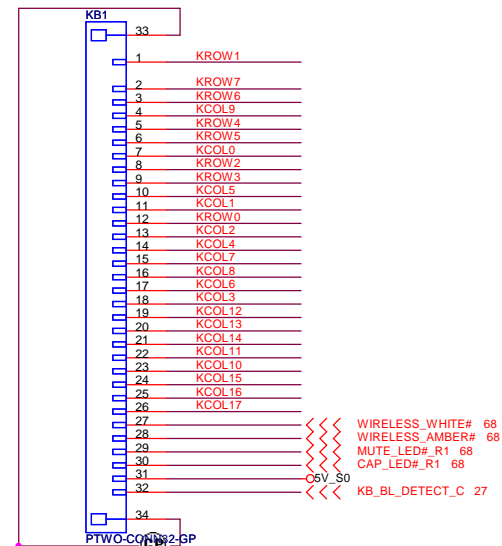
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103

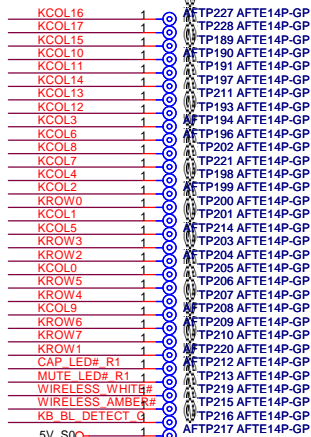
SSID = KBC

Internal KeyBoard Connector

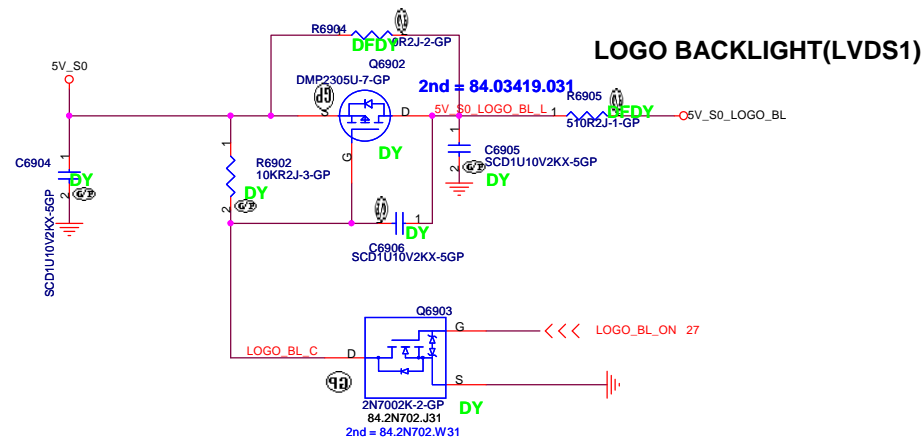


20.K0661.032
2nd = 20.K0660.032
3rd = 20.K0676.032

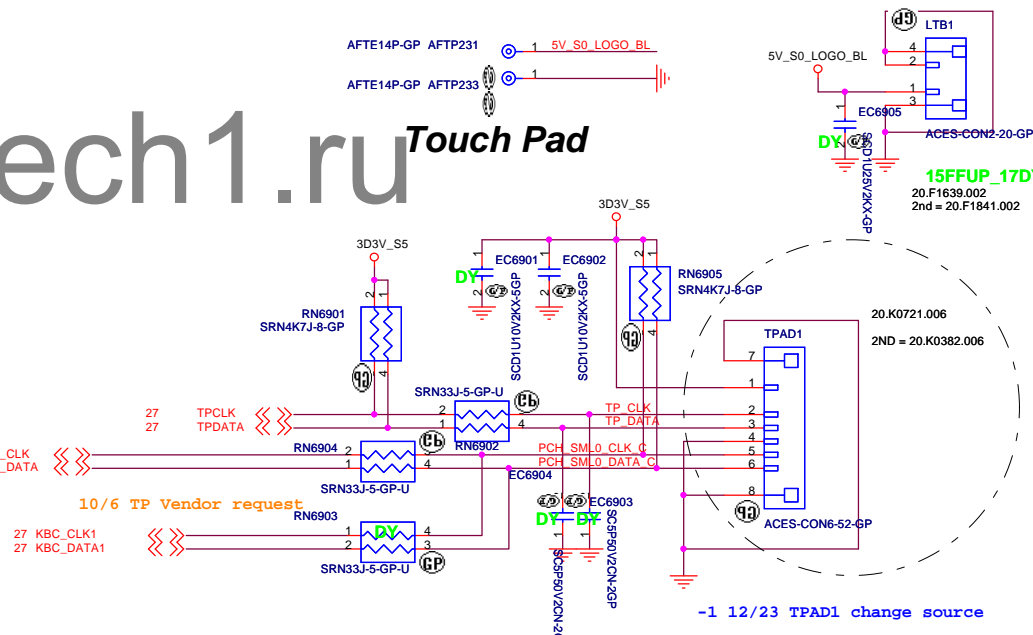
KB_BL_DETECT
HIGH = BL SKU
LOW = NON-BL SKU



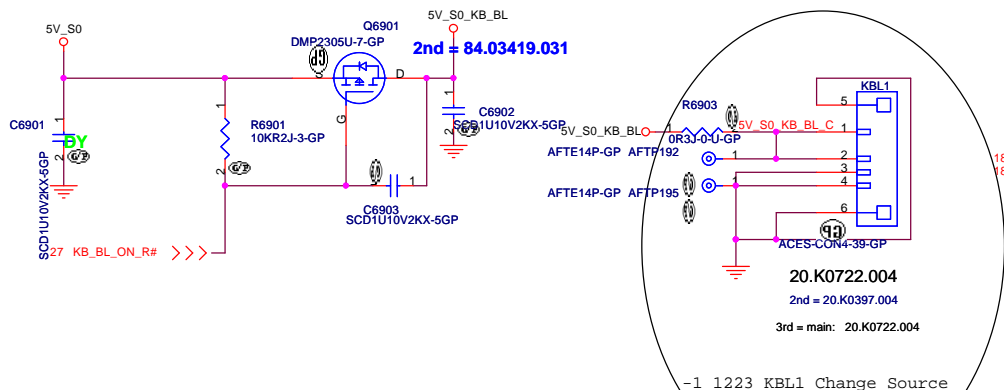
A Cover Logo Backlight



Touch Pad



Internal KeyBoard Backlight Connector



20.K0722.004
2nd = 20.K0397.004
3rd = main: 20.K0722.004

-1 1223 KBL1 Change Source

(Hall sensor at Power BD)

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Title

Hall Sensor

Size
A3

Document Number
Colossus

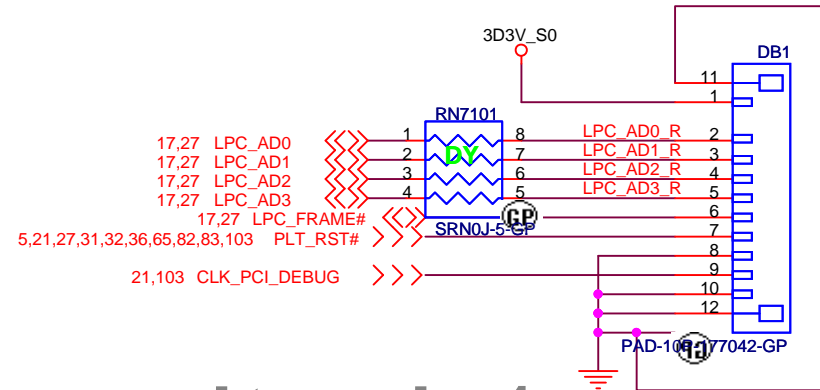
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DEBUG BD for Factory Test



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ZZ.00PAD.Y41

-1 0102

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Dubug connector

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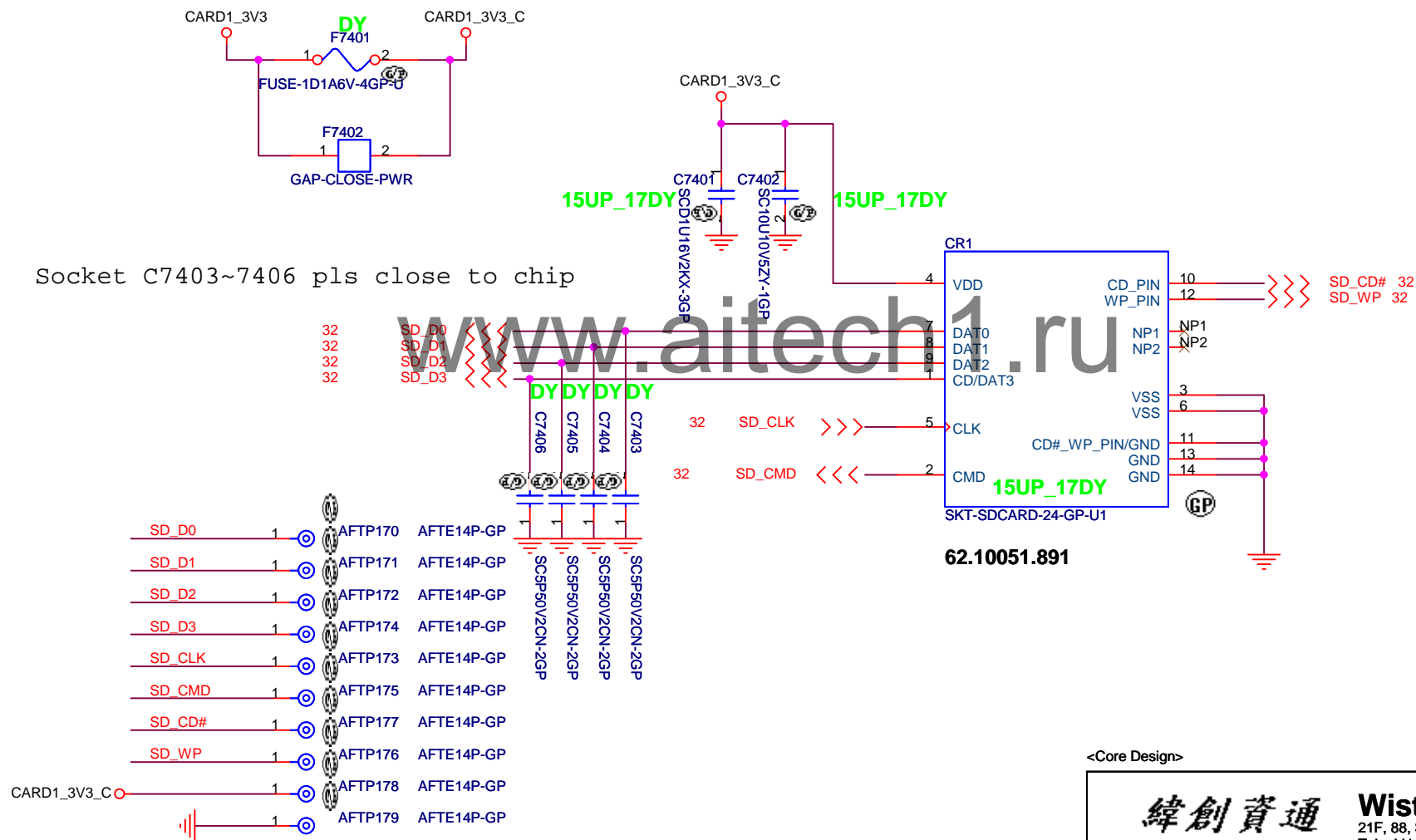
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2 IN1 CARD-READER (SD/MMC)



<Core Design>

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CARD Reader CONN

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Express Card

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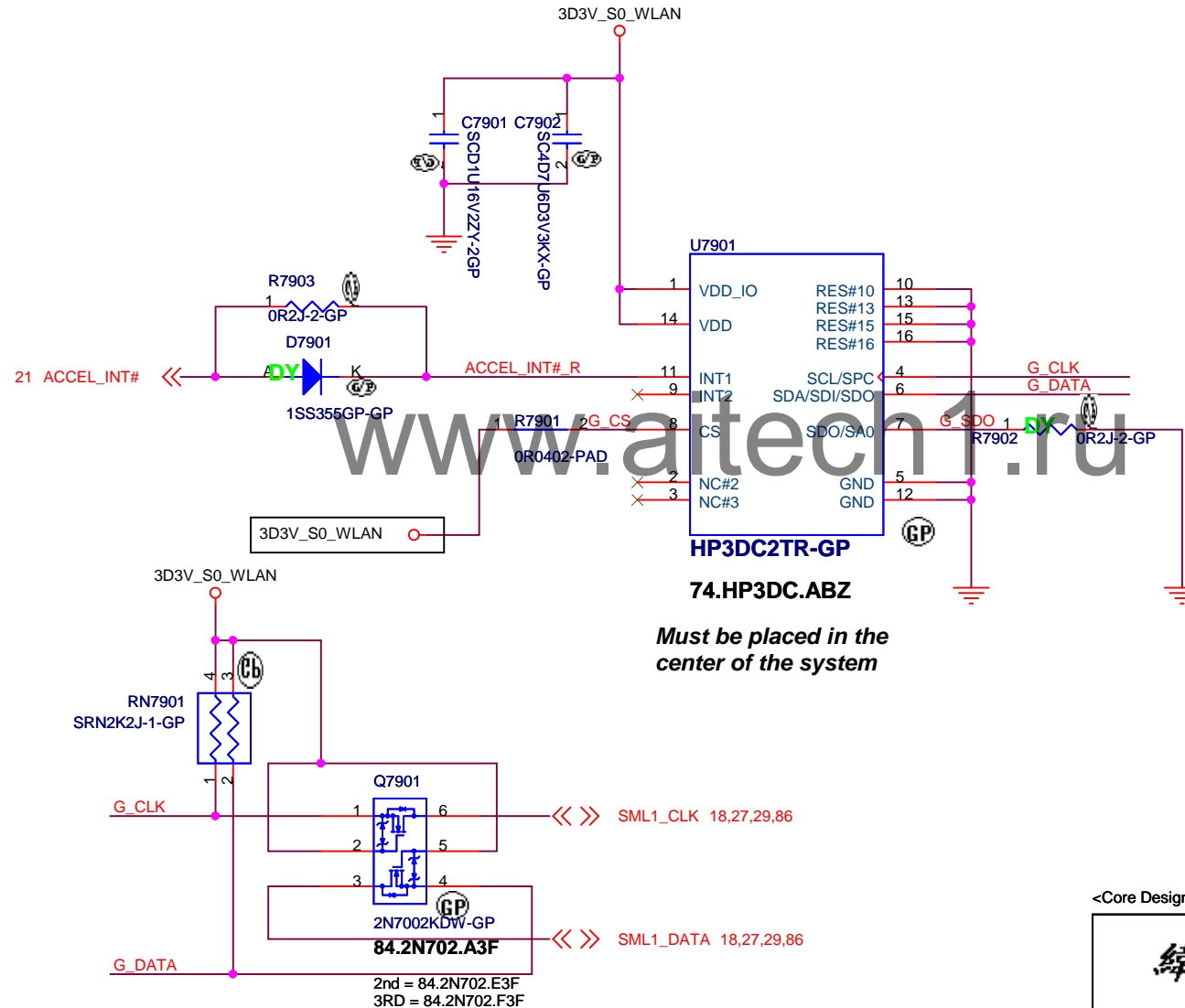
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ACCELEROMETER



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Title

ACCELEROMETER

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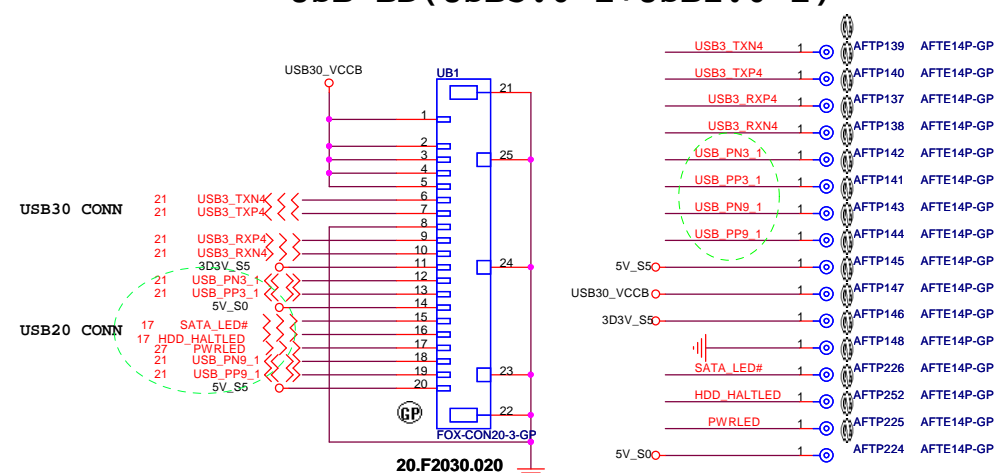
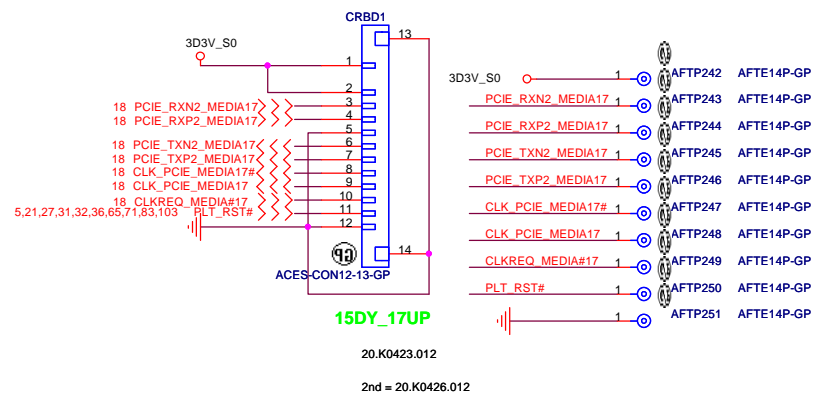
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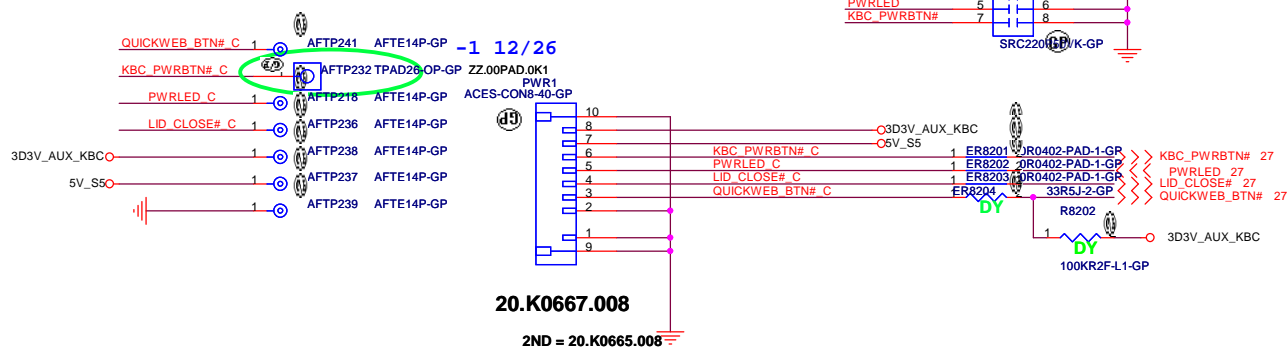
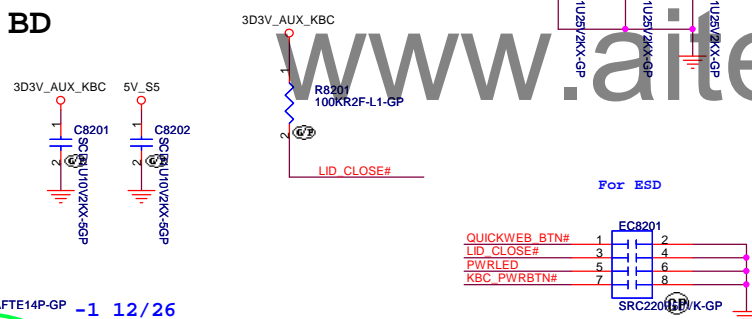
Card Reader BD 15"=DY

17"=PHASE IN

USB BD(USB3.0*1+USB2.0*1)

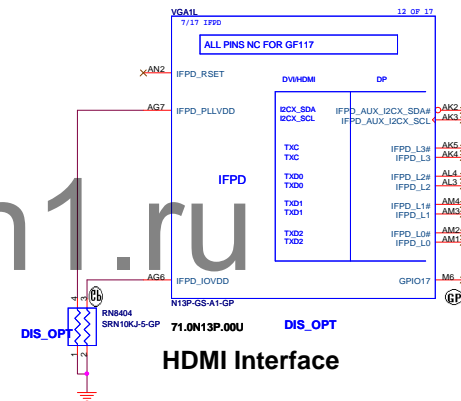
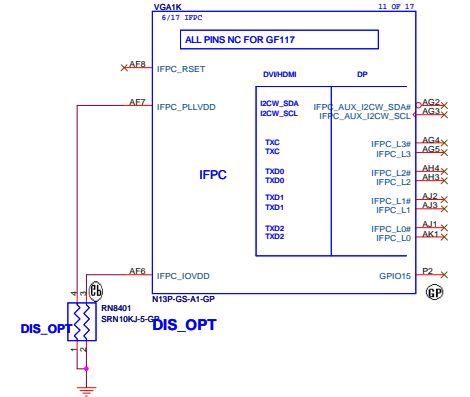
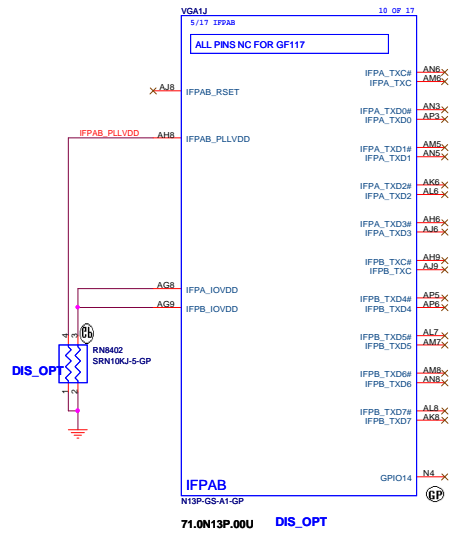


POWER BUTTON BD

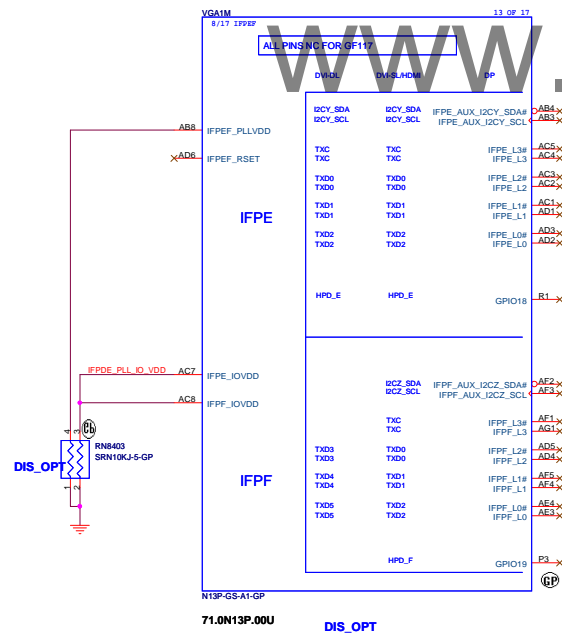


TOUCHPAD BD PAGE 69

LVDS Interface



HDMI Interface



VGA_CORE



<Variant Name>

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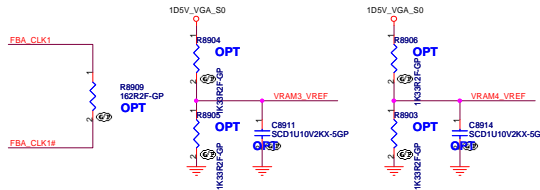
GPU DPPWR/GND(5/5)

Size Custom	Document Number Colossus	Rev 1
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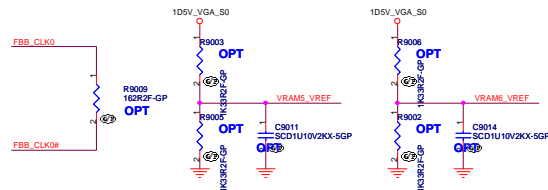
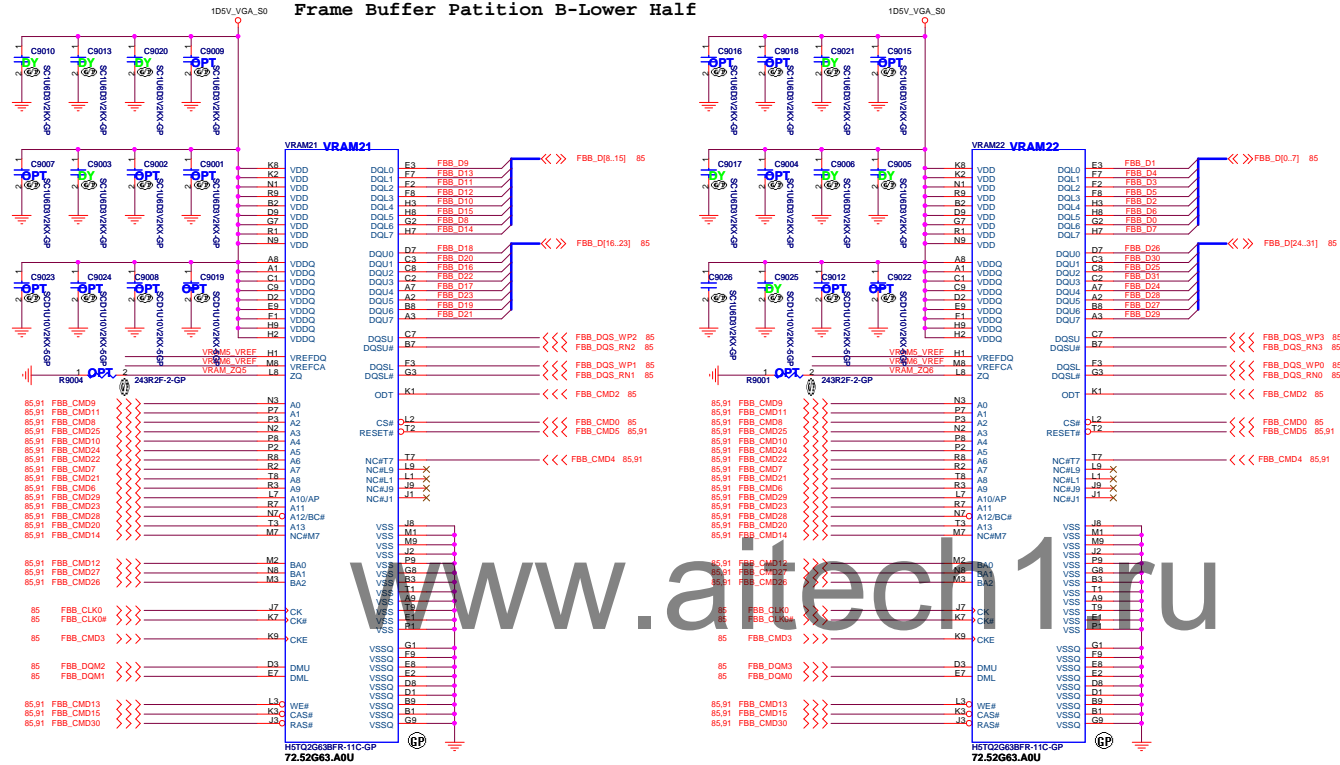


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Size A2	Document Number	Rev
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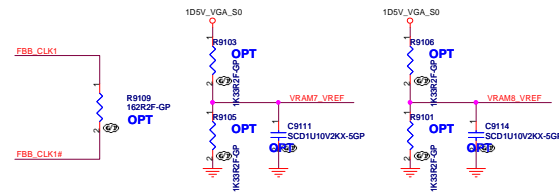
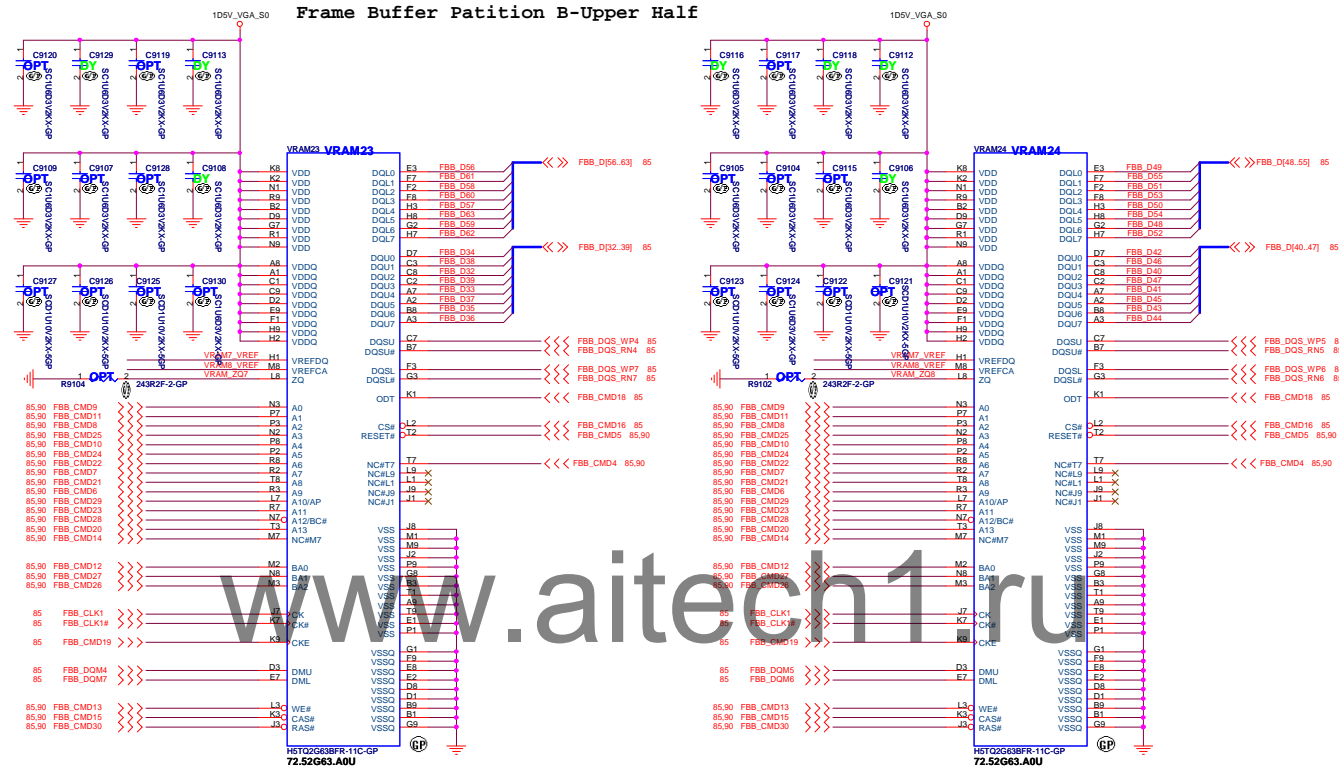
The diagram shows two signal traces, AITC12B# and AITC17#, with various timing points marked. The signals are active-low, indicated by the 'B#' and '17#' suffixes. The diagram includes labels for setup and hold times, and a large watermark 'www.aitech1.ru' is overlaid on the center.

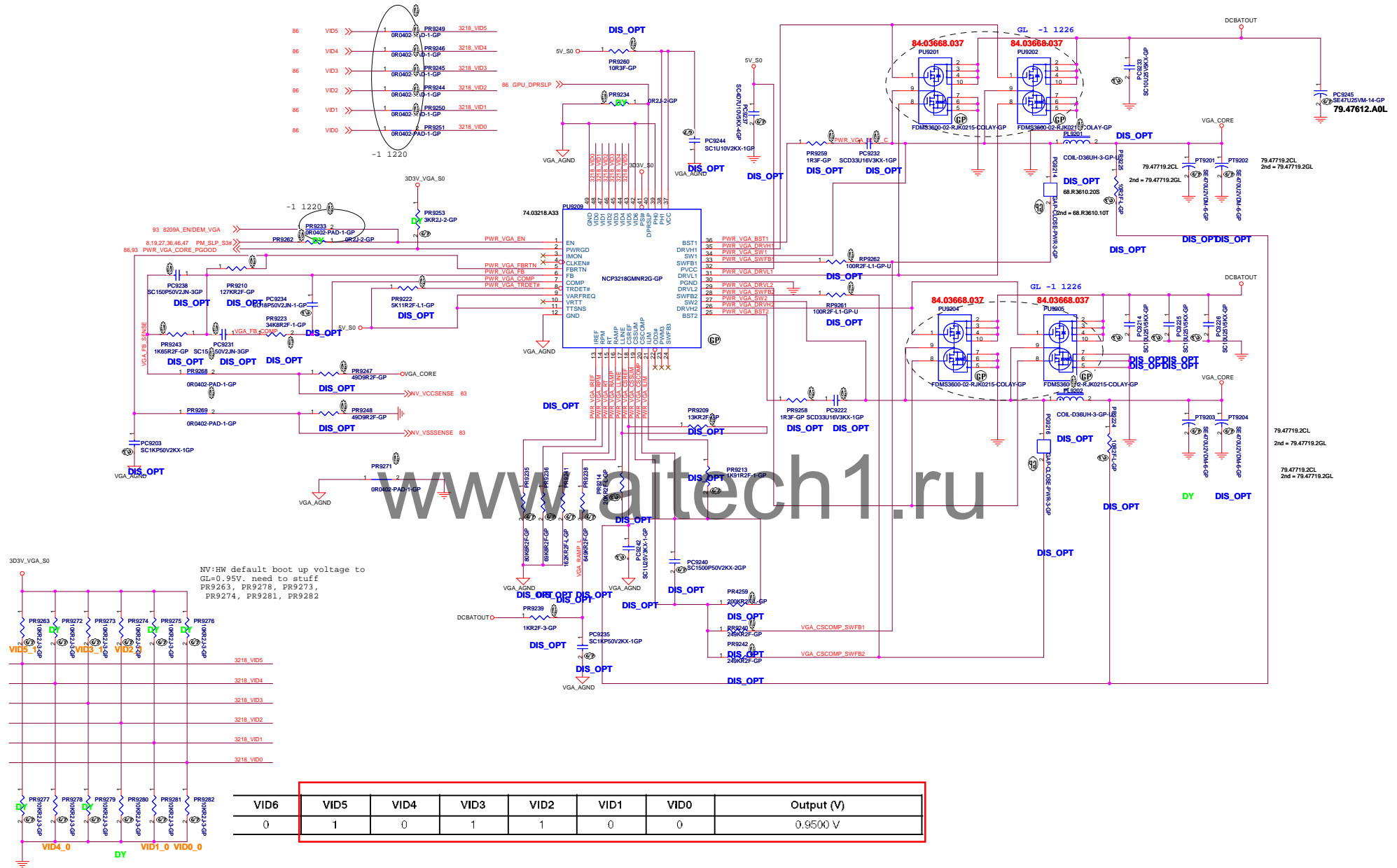


Frame Buffer Patition B-Lower Half



Frame Buffer Patition B-Upper Half





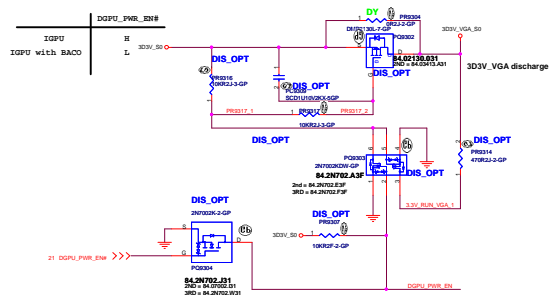
Core Design

VGA chip sequence: 3V_VGA_S0>VGA_CORE>1D5V_VGA>1D05V_VGA

3V_VGA_S0

VGA_CORE

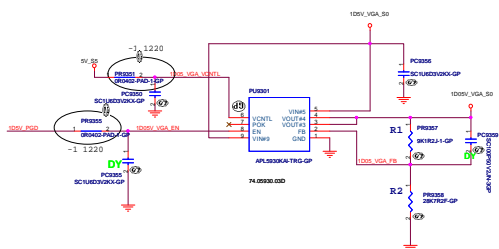
1.5V_VGA_S0



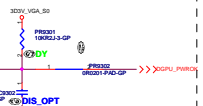
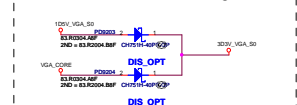
1D05V_VGA

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1D5V_VGA_S0
1D5V_VGA_S0 should ramp up
so 1D05V_VGA_S0 EN have to fine tune RC delay
after VGA_Core

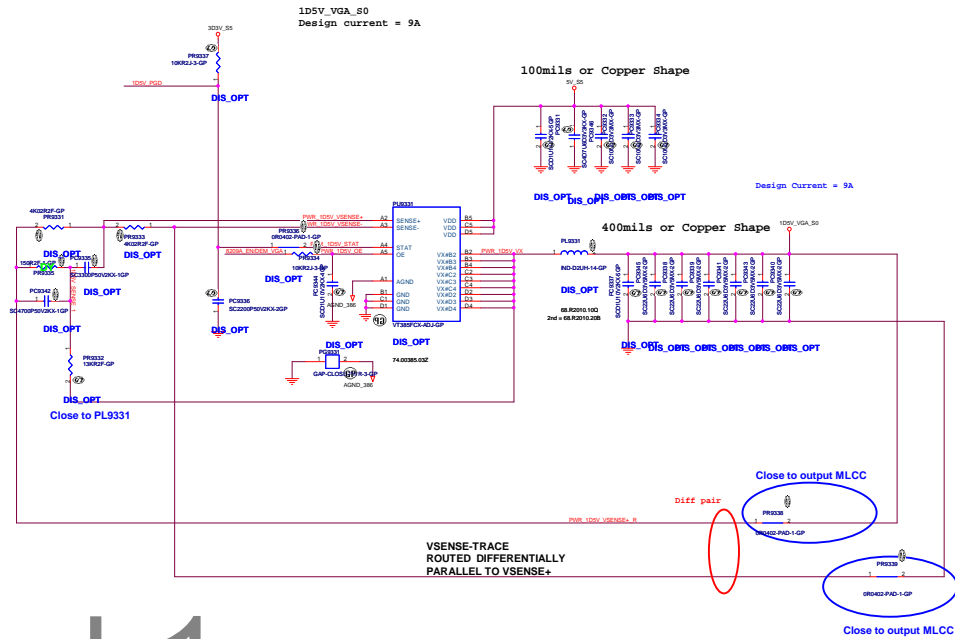
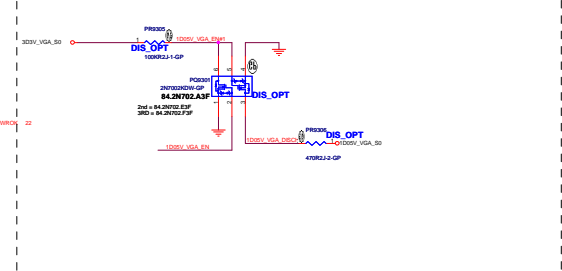
1D05V_VGA_S0
Design current = 3.8A



Discharge Circuit



Discharge Circuit



1D5V_VGA_S0
Design current = 9A

100mils or Copper Shape

Design Current = 9A

400mils or Copper Shape

Close to output MLCC

Diff pair

VSENSE-TRACE
ROUTED DIFFERENTIALLY
PARALLEL TO VSENSE+

Close to output MLCC

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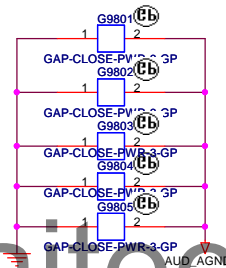
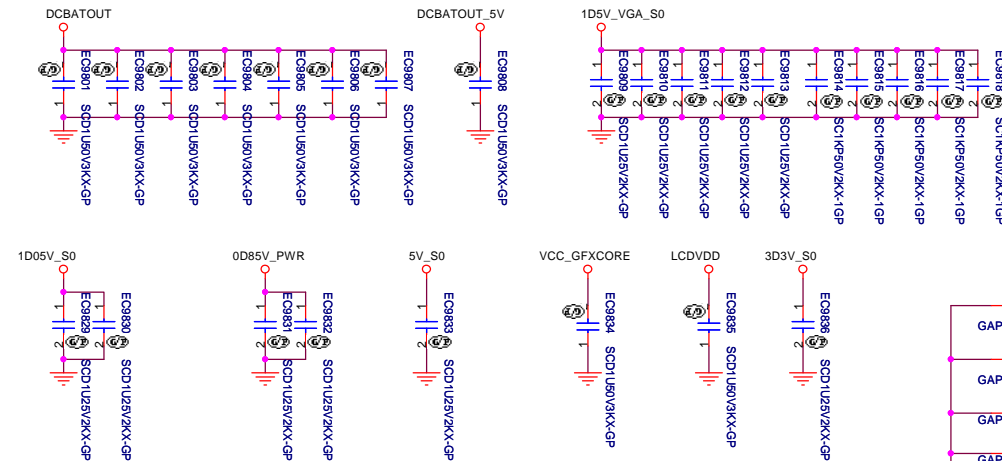
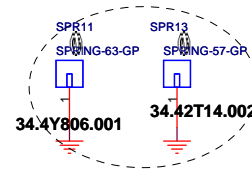
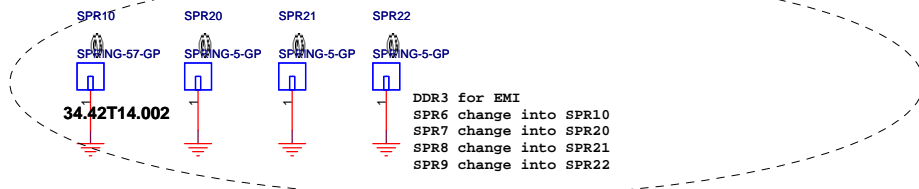
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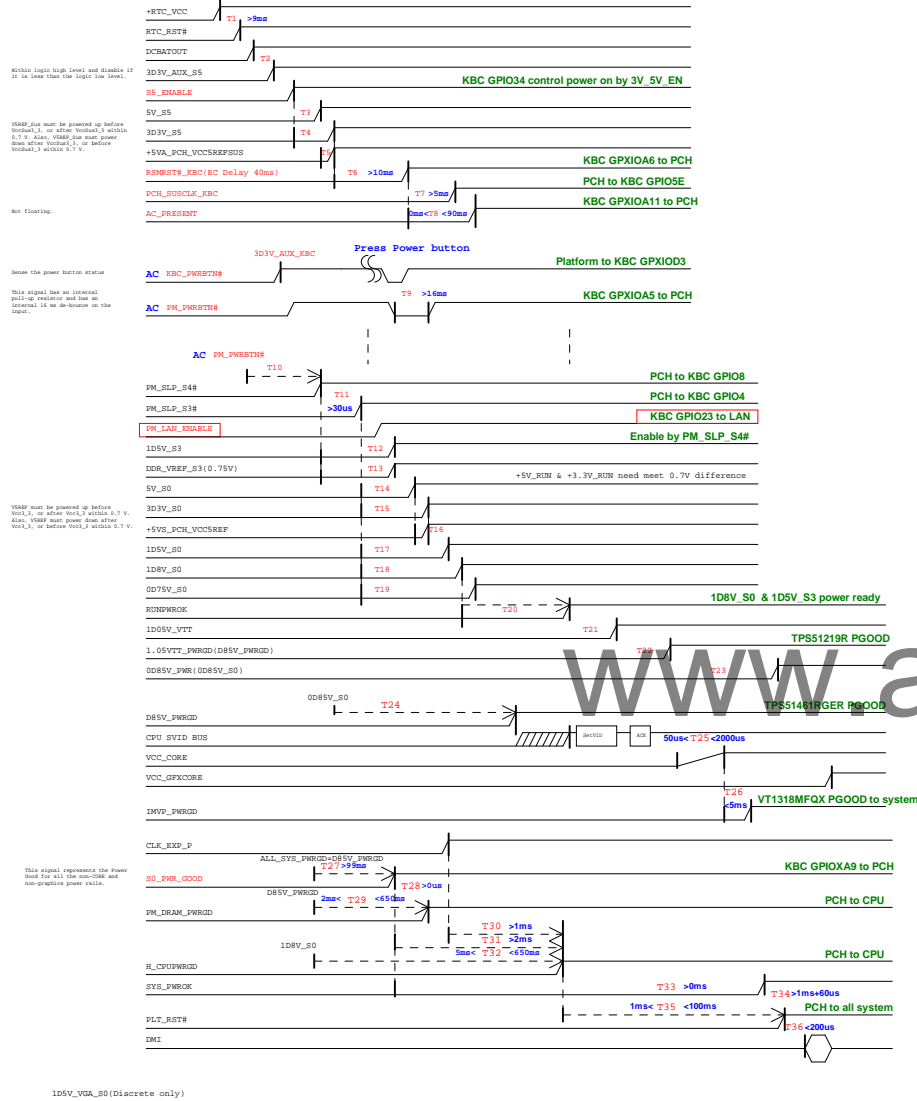
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 Taipei Hsien 221, Taiwan, R.O.C.

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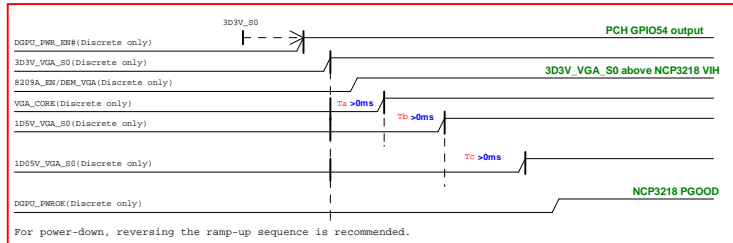
Chief River Platform Power Sequence

(AC mode)

red word: KBC GPIO



N13P Power-Up/Down Sequence



(DC mode)

red word: KBC GPIO

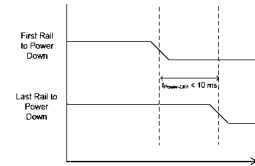
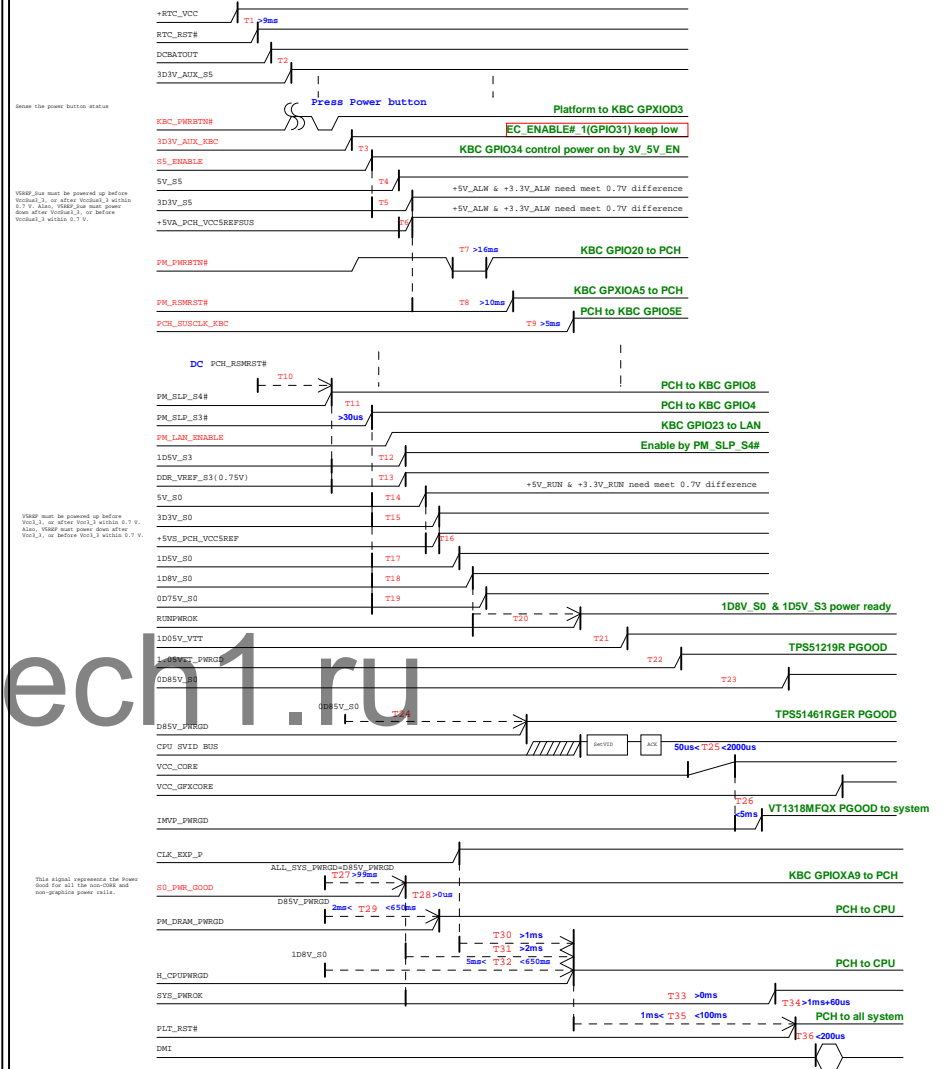
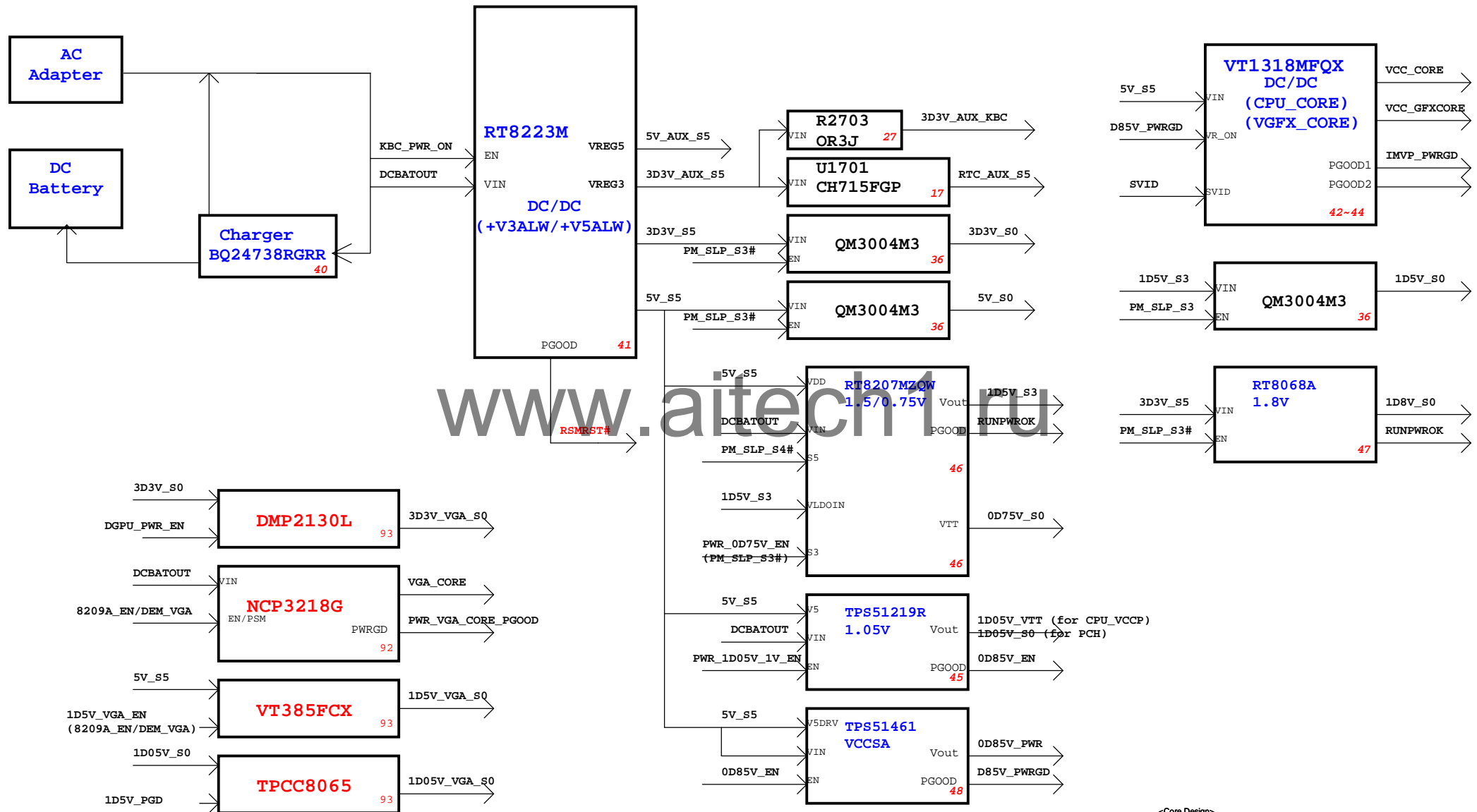
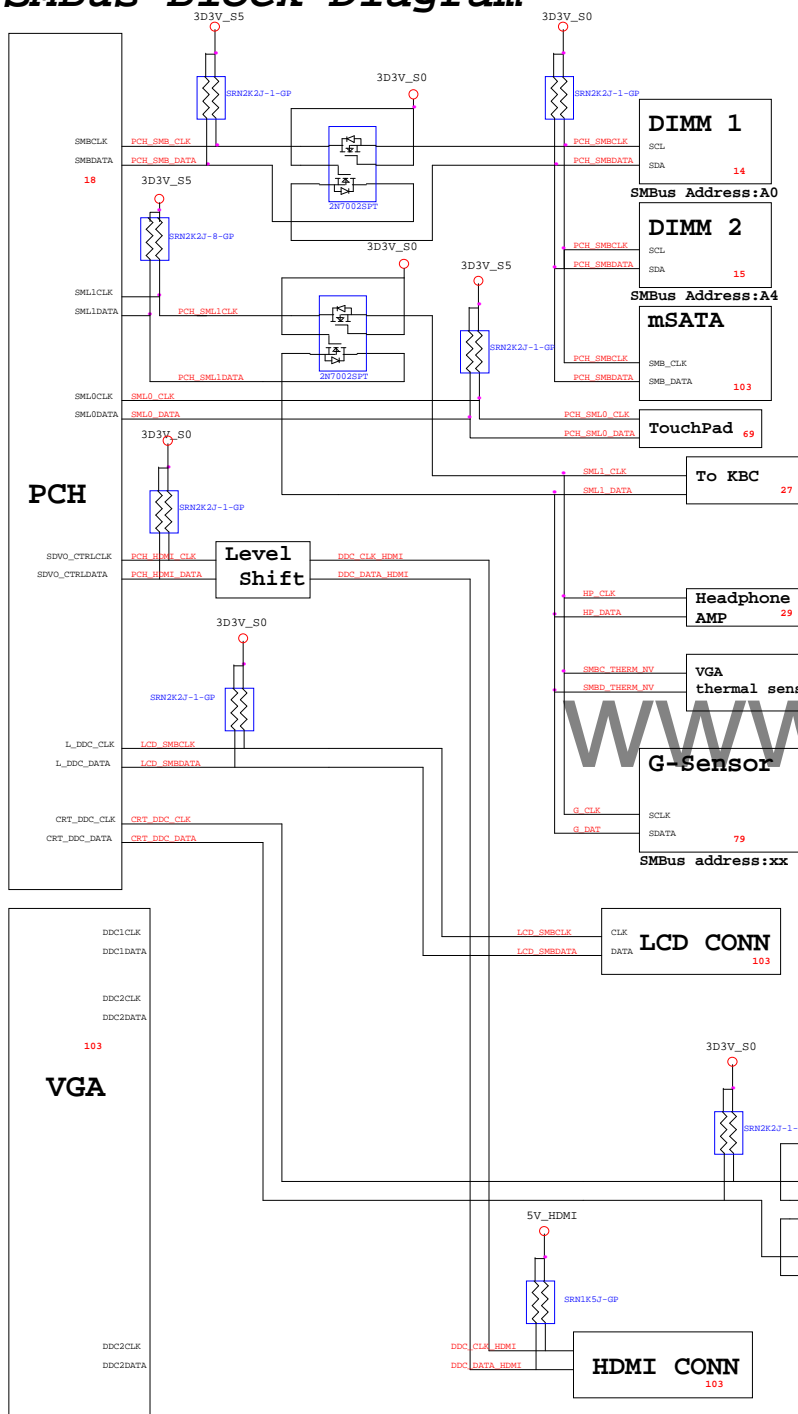


Figure 18. Recommended Power Off Sequencing Order

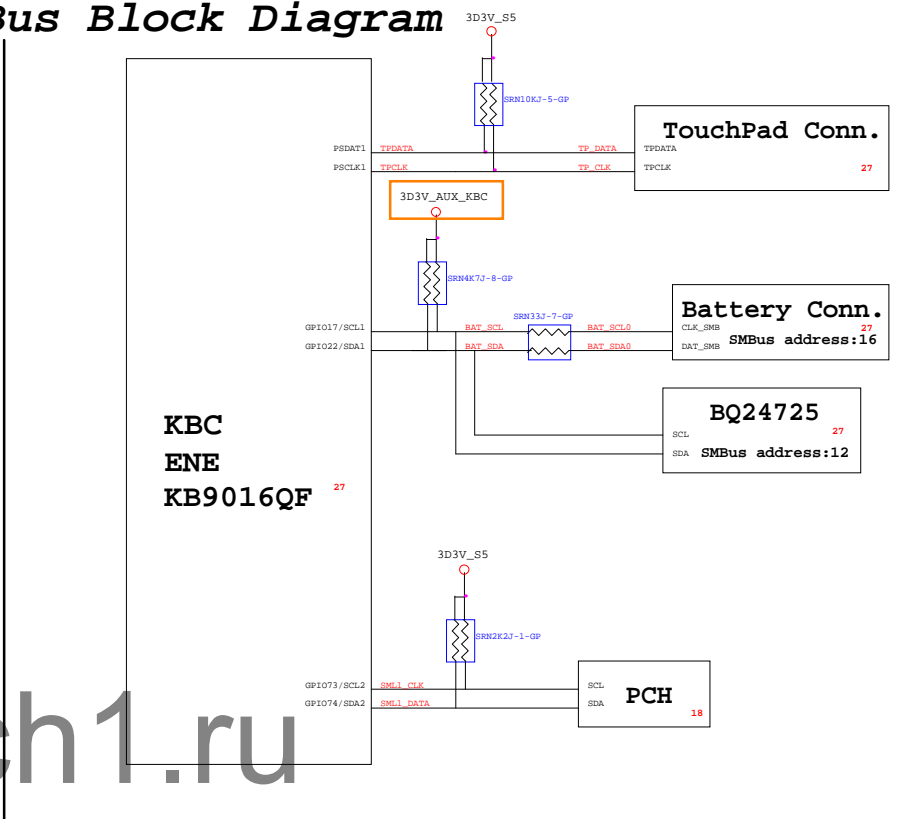
COLOSUSS POWER BLOCK DIAGRAM



PCH SMBus Block Diagram

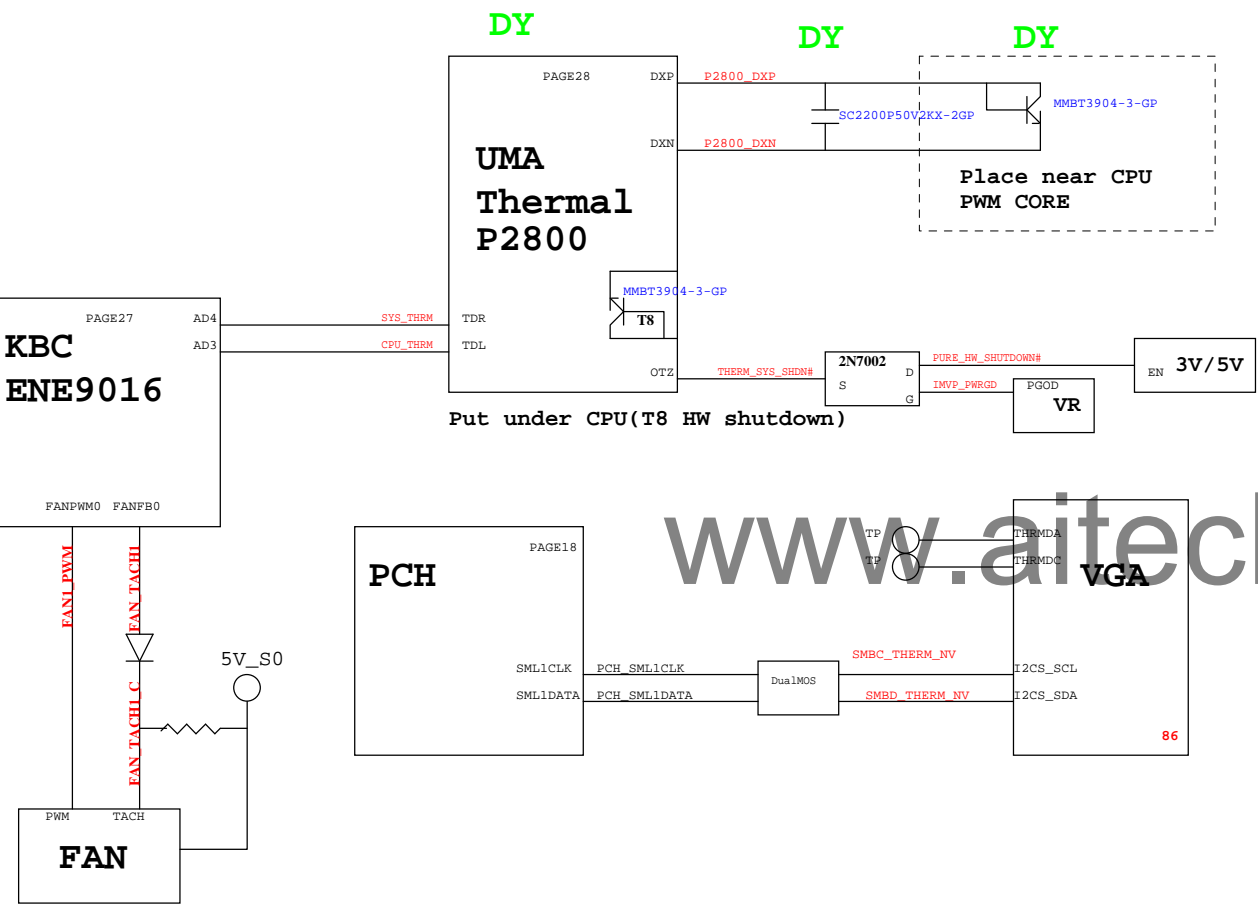


KBC SMBus Block Diagram

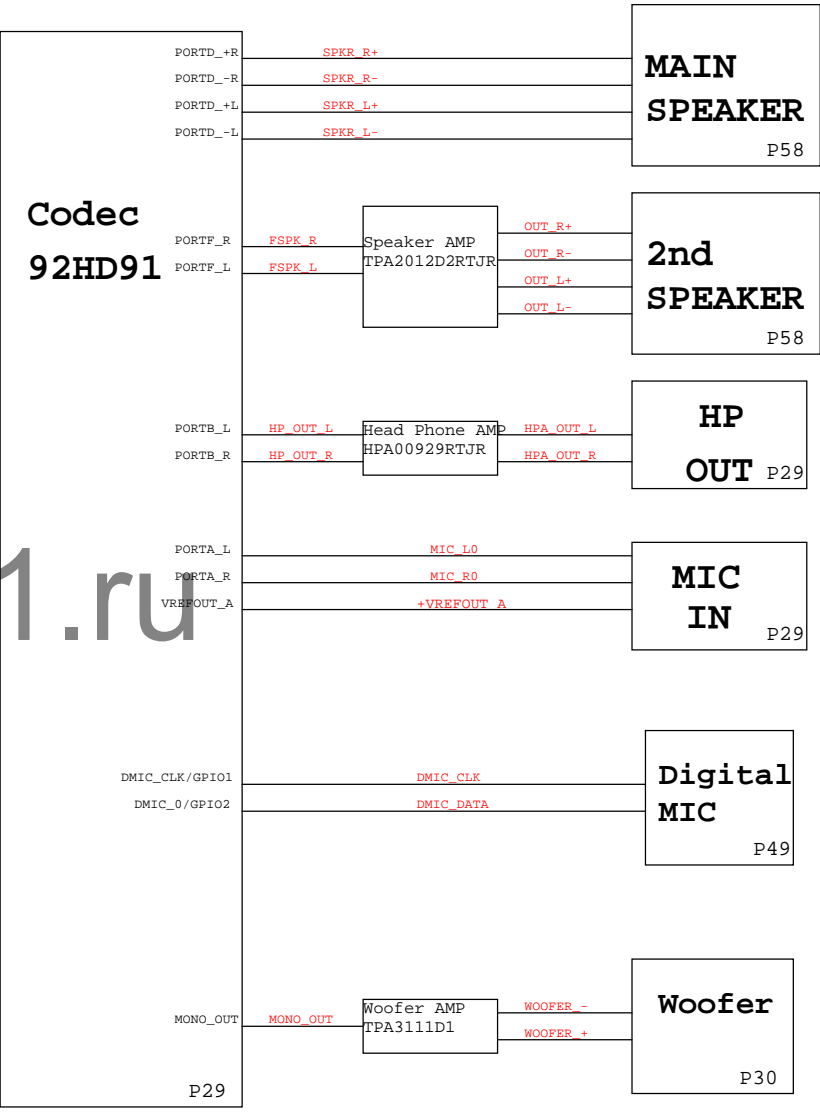


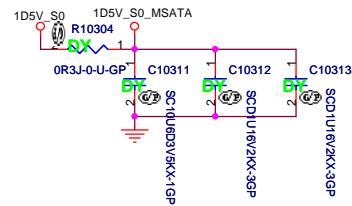
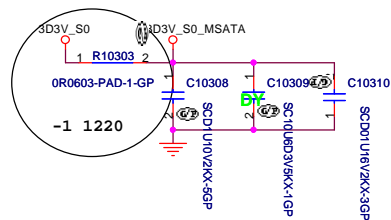
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Thermal Block Diagram

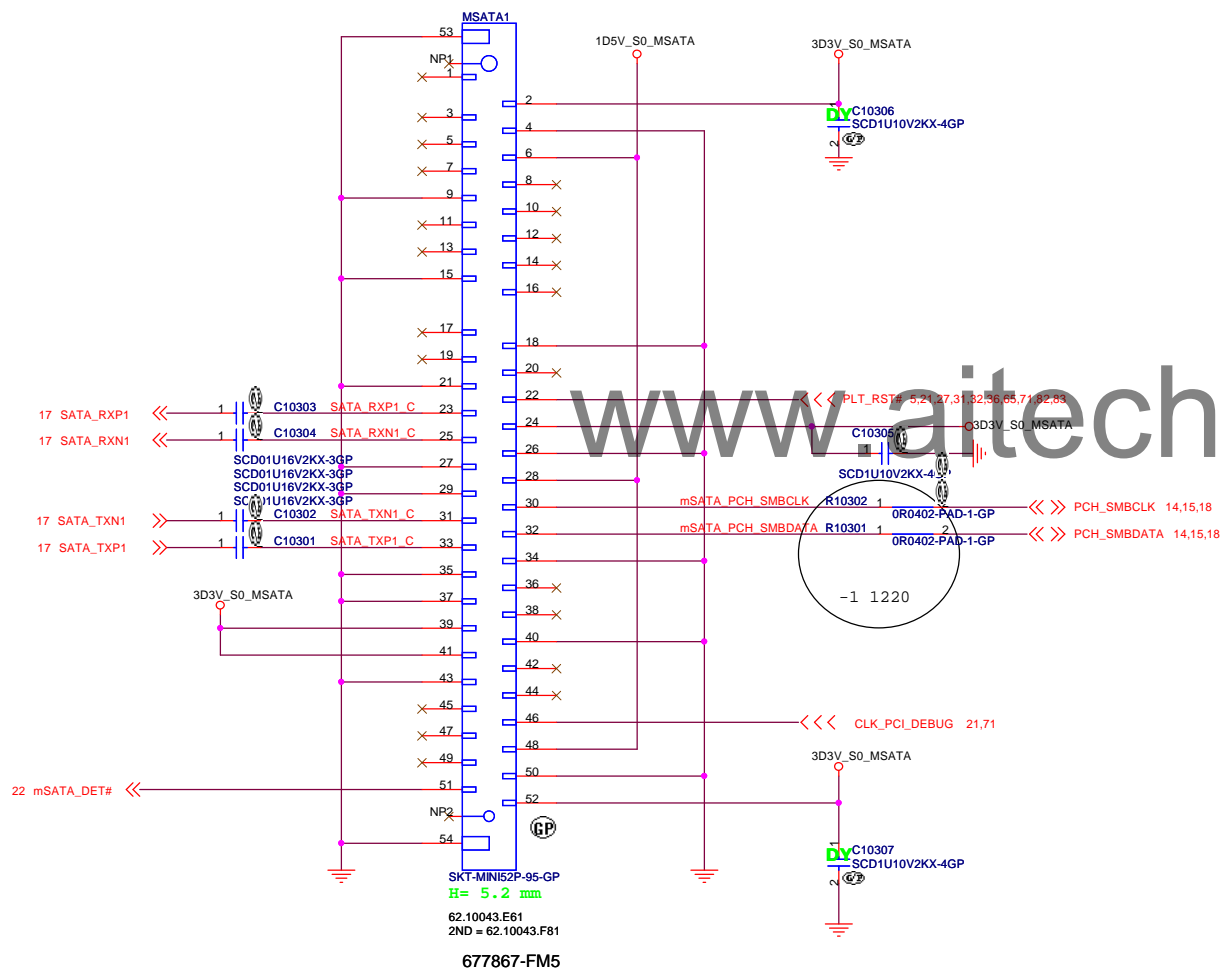


Audio Block Diagram





mSATA



Pin #	Name	Description	Pin #	Name	Description
1	Reserved	NC	2	V33	3.3V power
3	Reserved	NC	4	GND	Return Current Path
5	Reserved	NC	6	V15	1.5V power (Unused)
7	Reserved	NC	8	Reserved	NC
9	GND	Return Current Path	10	Reserved	NC
11	Reserved	NC	12	Reserved	NC
13	Reserved	NC	14	Reserved	NC
15	GND	Return Current Path	16	Reserved	NC
Key					
17	Reserved	NC	18	GND	Return Current Path
19	Reserved	NC	20	Reserved	NC
21	GND	Return Current Path	22	Reserved	NC
23	B+	Differential Signal Pair B (Device Tx)	24	V33	3.3V power
25	B-	Differential Signal Pair B (Device Tx)	26	GND	Return Current Path
27	GND	Return Current Path	28	V15	1.5V power (Unused)
29	GND	Return Current Path	30	Reserved	NC
31	A-	Differential Signal Pair A (Device Rx)	32	Reserved	NC
33	A+	Differential Signal Pair A (Device Rx)	34	GND	Return Current Path
35	GND	Return Current Path	36	Reserved	NC
37	GND	Return Current Path	38	Reserved	NC
39	V33	3.3V power	40	GND	Return Current Path
41	V33	3.3V power	42	Reserved	NC
43	GND	Return Current Path	44	Reserved	NC
45	Vendor	No connect at Host side	46	Reserved	NC
47	Vendor	No connect at Host side	48	V15	1.5V power (Unused)
49	DAS/DSS	Drive Activity Signal	50	GND	Return Current Path
51	Presense	Device Presense	52	V33	3.3V power

Note: 1: DAS/DSS signal is not use for this drive. (DAS Signal output is optional)

*2: Presense pin is Connected to GND by device side. (220 Ω Pull Down)

1st 677867-FM5
2nd 677867-AM5
3rd 677867-BM5
4th 677867-LM5

<Core Design>

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mSATA

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